Test Driven Design

Results

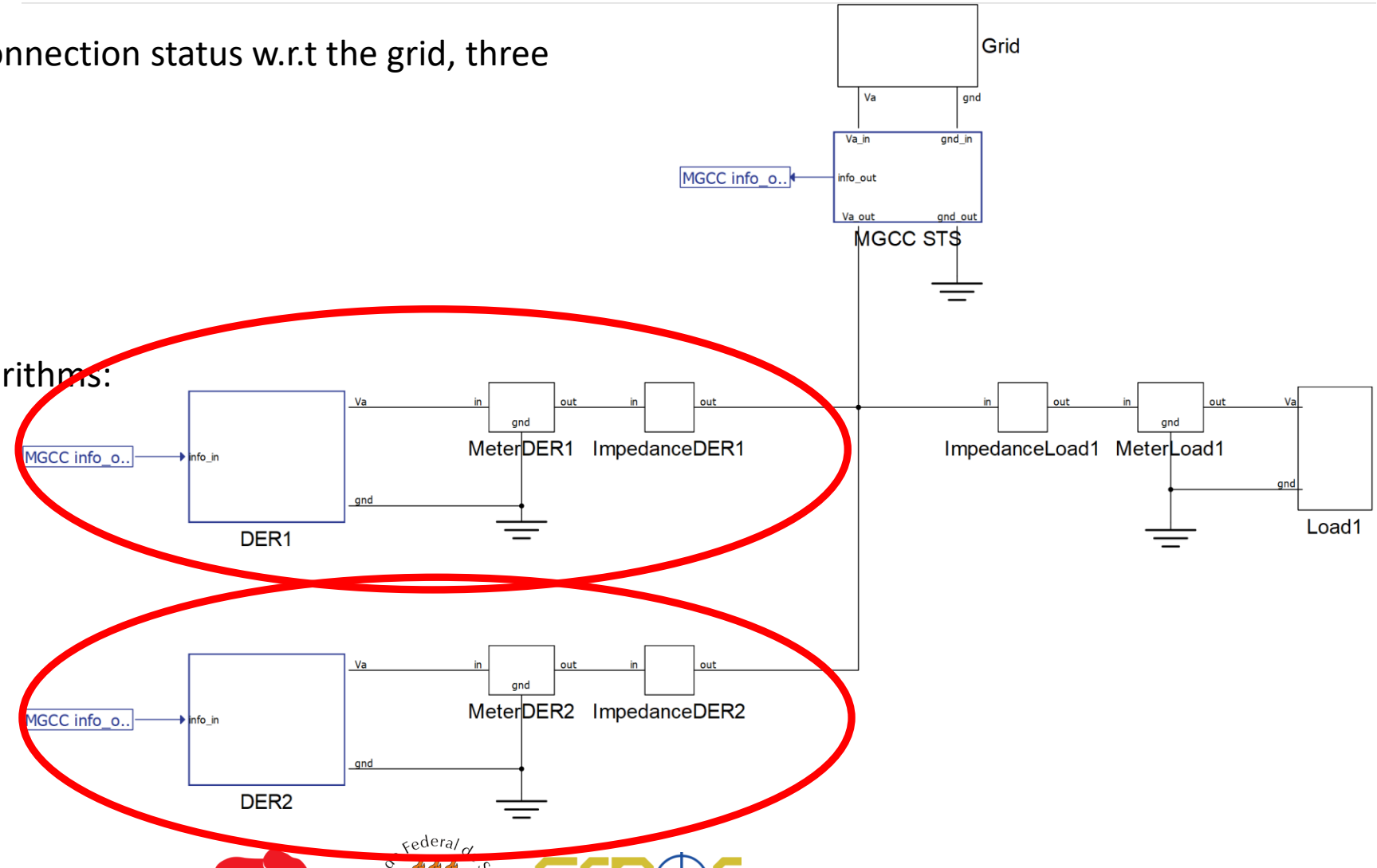
Case Studies

According the DER's 1 and 2 connection status w.r.t the grid, three cases were simulated:

- ☑ Grid-connected Mode;
- ☑ Transition Mode and
- ☑ Islanded Mode.

Evaluated primary control algorithms:

- ❑ Droop control;
- ❑ 2I Droop control;
- ❑ dVOC;
- ❑ VSG 1 control and
- ❑ VSG 2 control



Typhoon HIL

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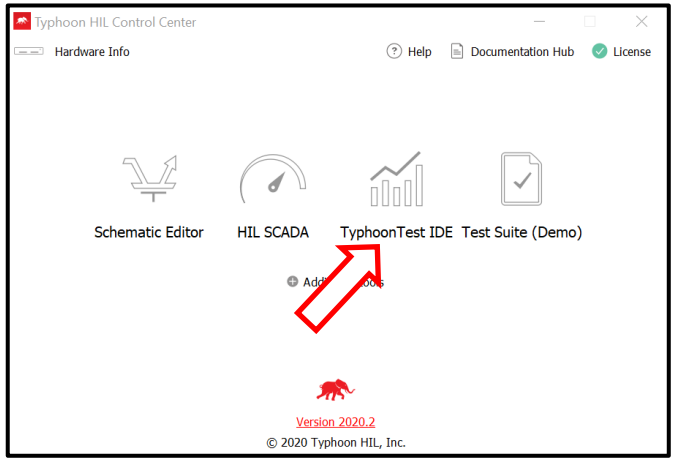
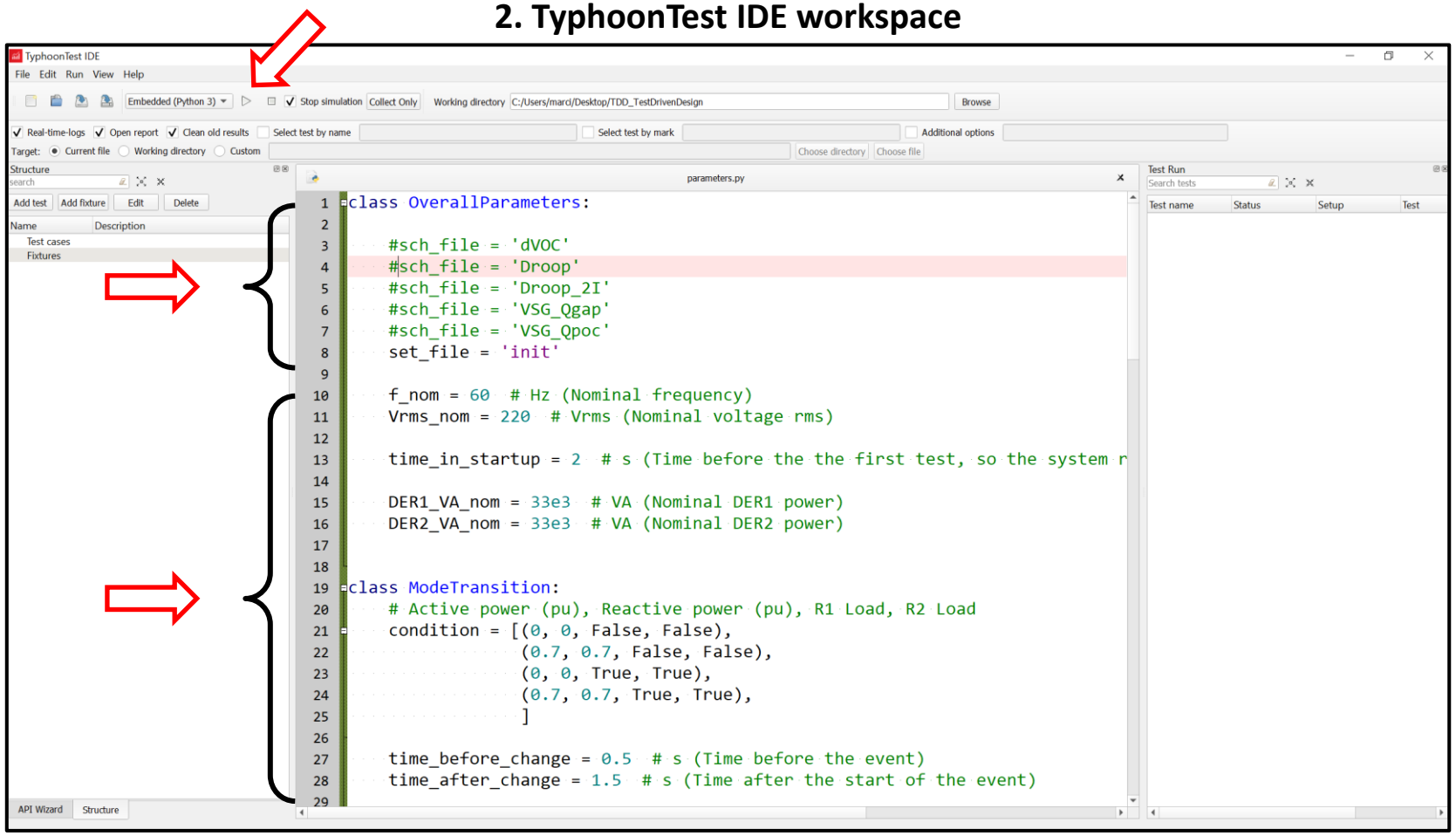
Test-driven Development (TDD) at a Glance

1. Typhoon HIL Control Center panel



2. TyphoonTest IDE workspace




```
class OverallParameters:

    #sch_file = 'dVOC'
    #sch_file = 'Droop'
    #sch_file = 'Droop_2I'
    #sch_file = 'VSG_Qgap'
    #sch_file = 'VSG_Qpoc'
    set_file = 'init'

    f_nom = 60  # Hz (Nominal frequency)
    Vrms_nom = 220  # Vrms (Nominal voltage rms)

    time_in_startup = 2  # s (Time before the the first test, so the system r

    DER1_VA_nom = 33e3  # VA (Nominal DER1 power)
    DER2_VA_nom = 33e3  # VA (Nominal DER2 power)


class ModeTransition:
    # Active power (pu), Reactive power (pu), R1 Load, R2 Load
    condition = [(0, 0, False, False),
                 (0.7, 0.7, False, False),
                 (0, 0, True, True),
                 (0.7, 0.7, True, True),
                 ]

    time_before_change = 0.5  # s (Time before the event)
    time_after_change = 1.5  # s (Time after the start of the event)
```

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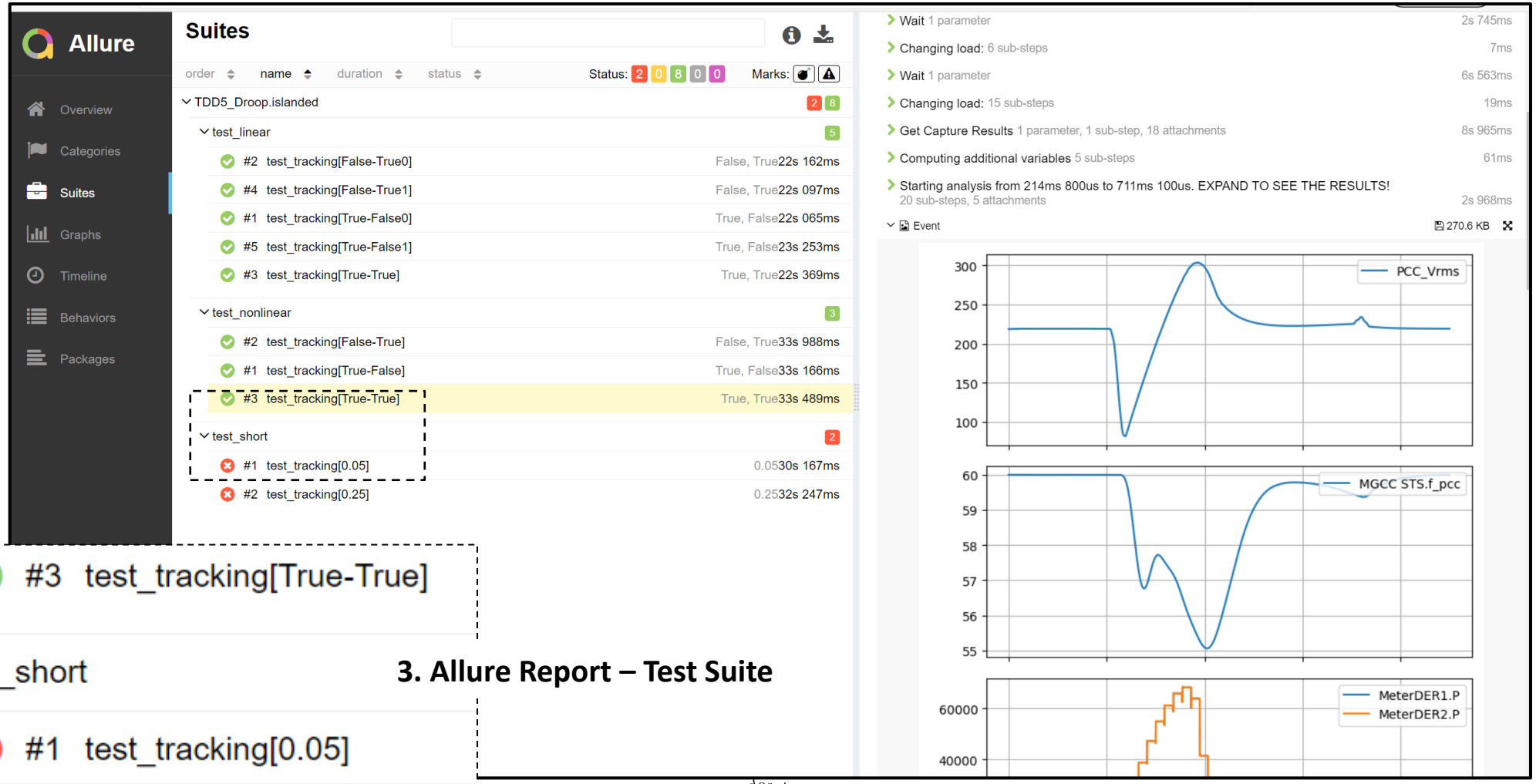
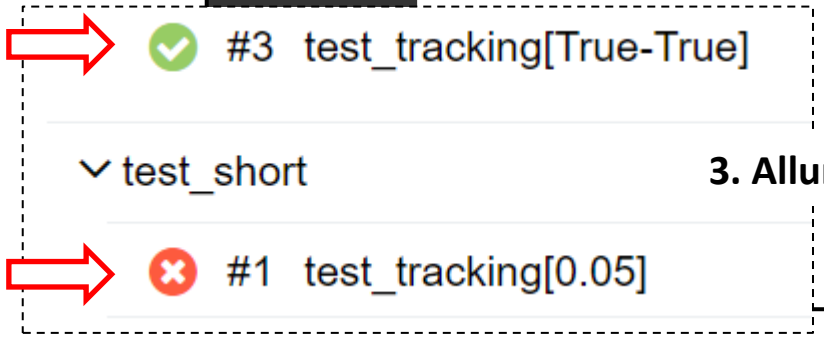
Test-driven Development (TDD) at a Glance





3. Allure Report – Test Suite

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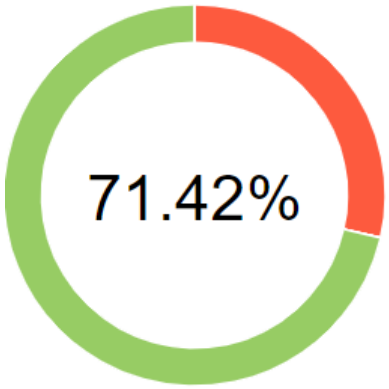
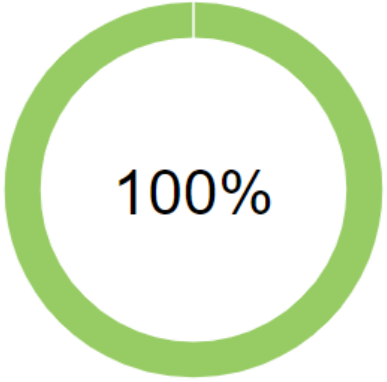
Grid-connected Dispatch Steady-State Tests

Performed tests:

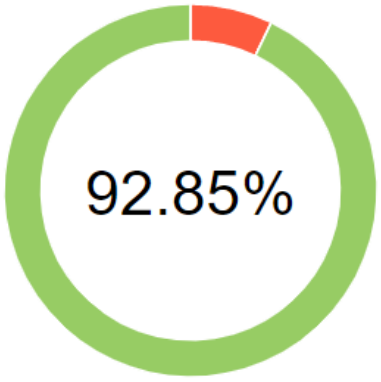
- ❑ Frequency Droop (grid frequencies: 57 Hz : 1 Hz ; 63 Hz)
- ❑ Voltage Droop (grid voltages: 200 V : 10 V : 240 V)



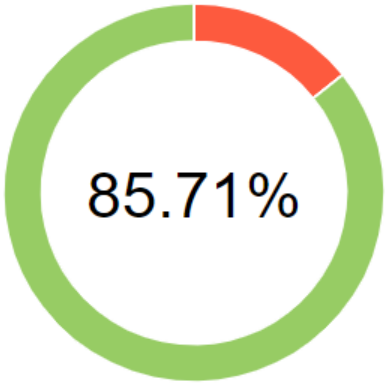
Droop



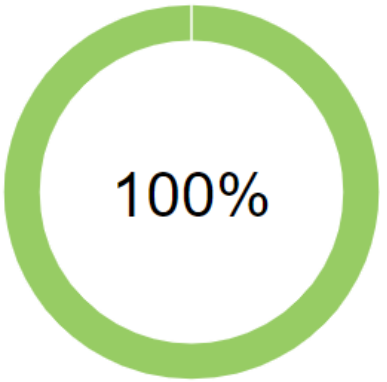
2I Droop



dVOC



VSG (Q_{gap})



VSG (Q_{poc})

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Grid-connected Dispatch Steady-State Tests

Thresholds

```python
class FrequencyDroop:
    f_range = [57, 58, 59, 60, 61, 62, 63]  # Hz (Frequency points to test the droop)
    Pref_range_pu = [0]  # W_pu (Active power reference during frequency condition)

    time_before_change = 0.2  # s (Time before the event)
    time_after_change = 2  # s (Time after the start of the event)

    desired_droop_pu = -0.334  # W_pu/Hz (Desired droop)

    # Thresholds:
    tolerance_pu = 0.15  # W (Acceptable active power tracking error in pu)
    max_ripple = 1  # W (Acceptable active power ripple)
```

```python
class VoltageDroop:
    Vrms_range = [200, 210, 220, 230, 240]  # Vrms (Voltage points to test the droop)
    Qref_range_pu = [0]  # VAr_pu (Reactive power reference during voltage condition)

    time_before_change = 0.2  # s (Time before the event)
    time_after_change = 2  # s (Time after the start of the event)

    desired_droop_pu = -0.0455  # VAr_pu/V (Desired droop)

    # Thresholds:
    tolerance_pu = 0.15  # VAr (Acceptable reactive power tracking error in pu)
    max_ripple = 1  # VAr (Acceptable reactive power ripple)
```

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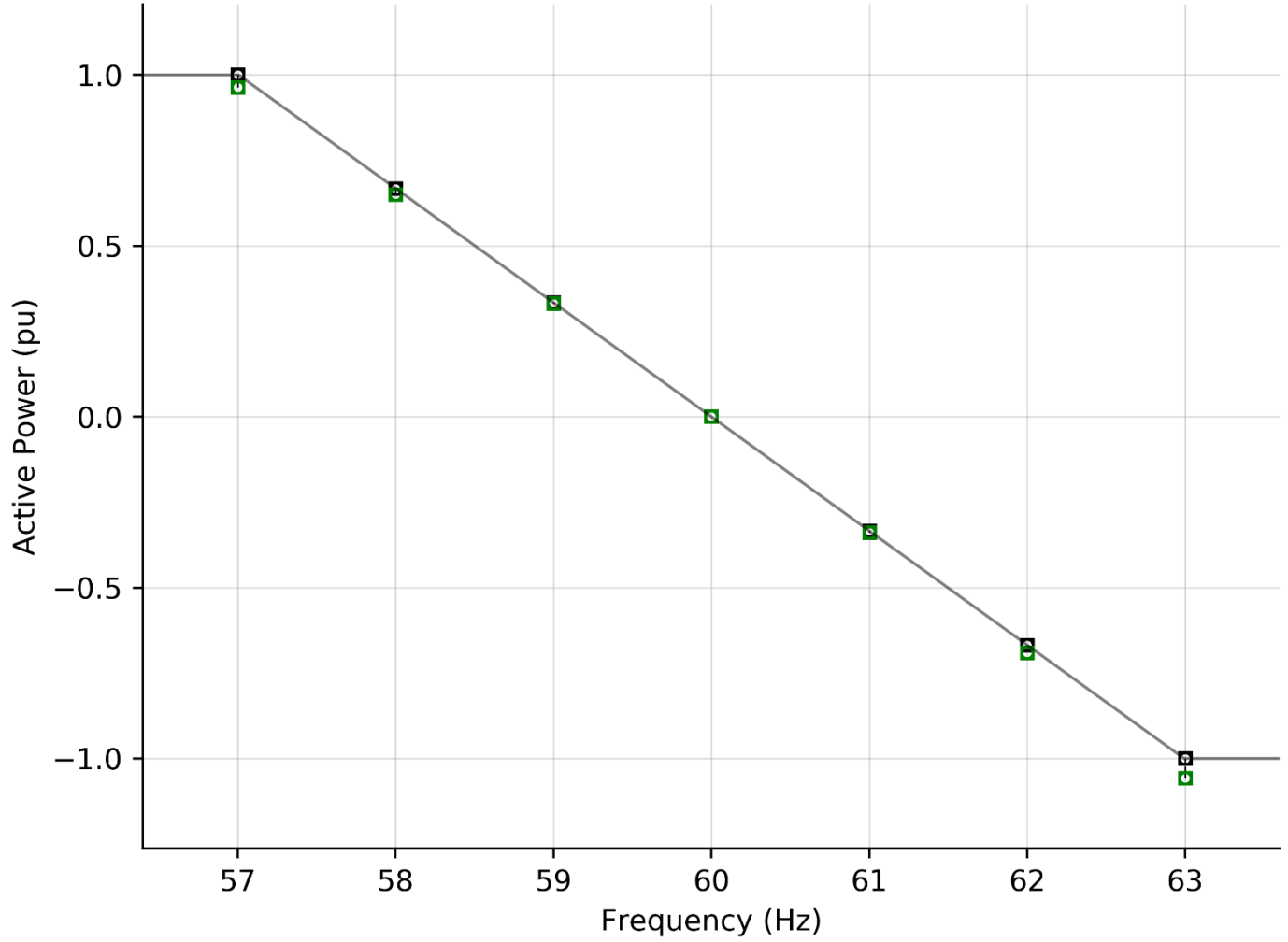
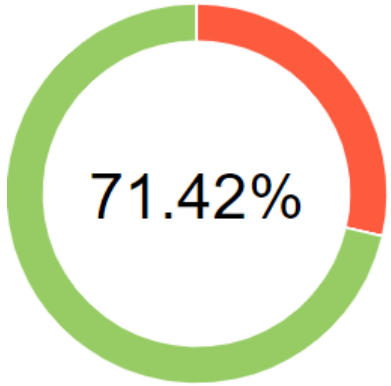
Droop control





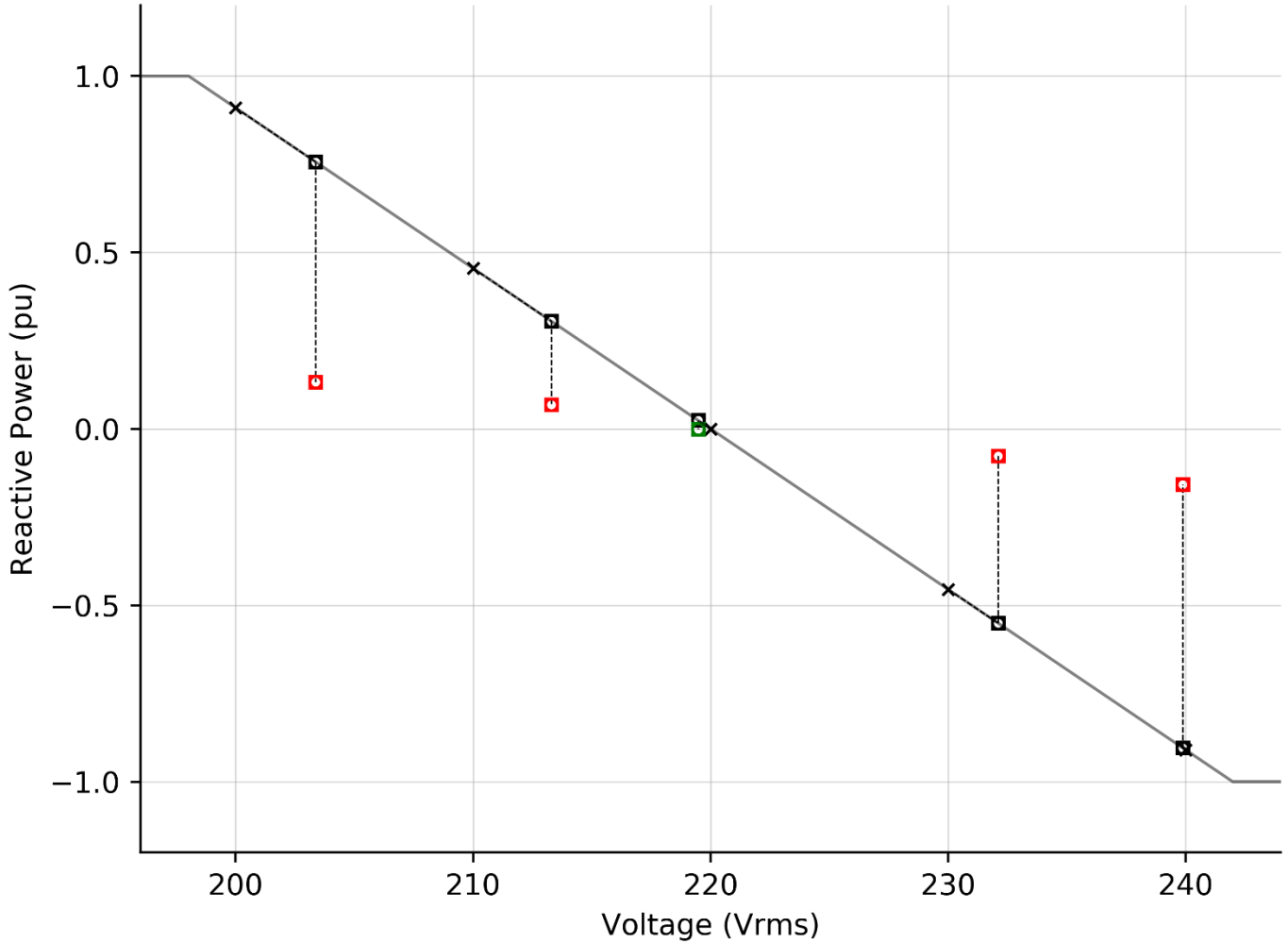
test_01_droop_frequency

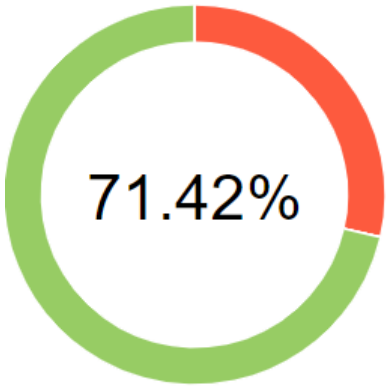
- #1 test_droop[0-57]
- #2 test_droop[0-58]
- #3 test_droop[0-59]
- #4 test_droop[0-60]
- #5 test_droop[0-61]
- #6 test_droop[0-62]
- #7 test_droop[0-63]

$DER1_{exp}$ $DER1_{avg}Fail$ $DER1_{avg}Ok$ $DER2_{avg}Ok$ Connection

$DER2_{exp}$ $DER2_{avg}Fail$

Droop control





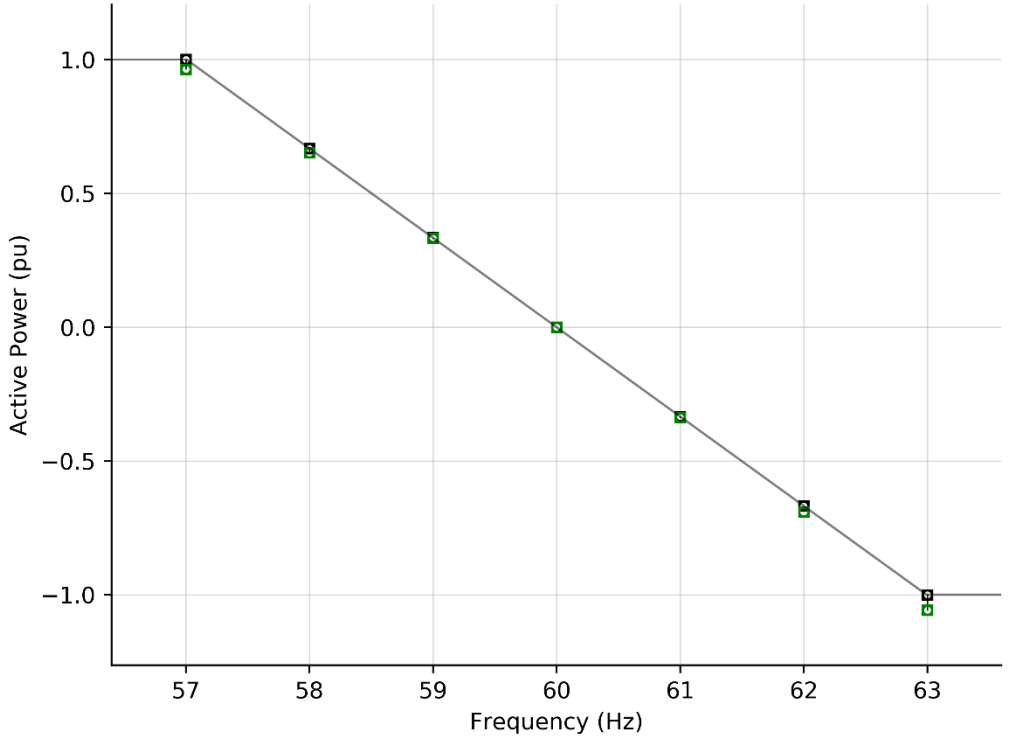
test_02_droop_voltage

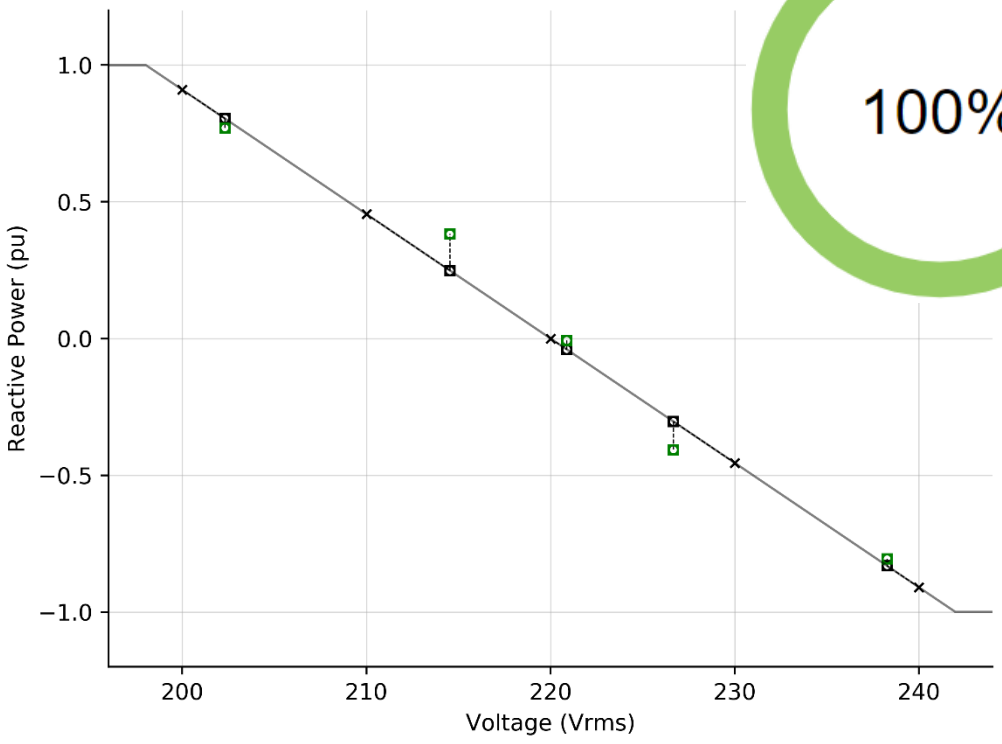
- #1 test_droop[0-200]
- #2 test_droop[0-210]
- #3 test_droop[0-220]
- #4 test_droop[0-230]
- #5 test_droop[0-240]

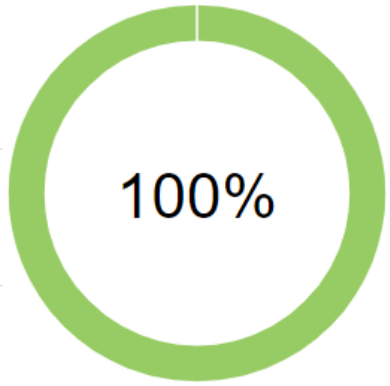
Org_{exp} $DER2_{exp}$ $DER2_{avg}Fail$ $DER2_{avg}Ok$ Connection

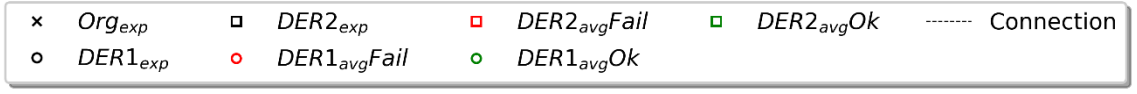
$DER1_{exp}$ $DER1_{avg}Fail$ $DER1_{avg}Ok$

2I-Droop control

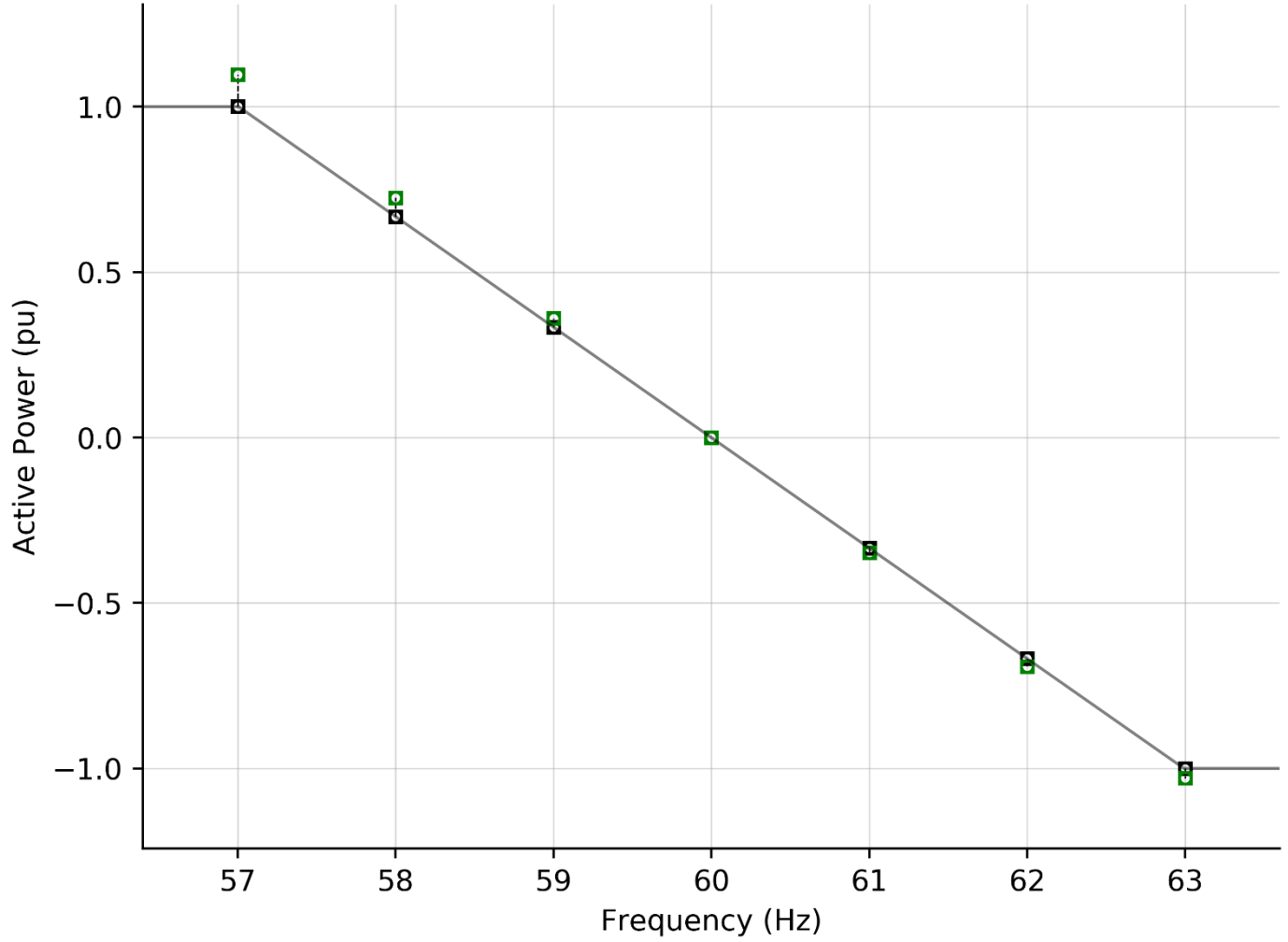


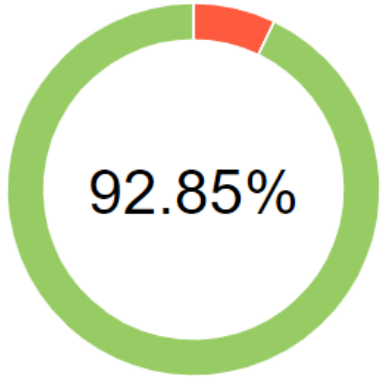






dVOC





test_01_droop_frequency

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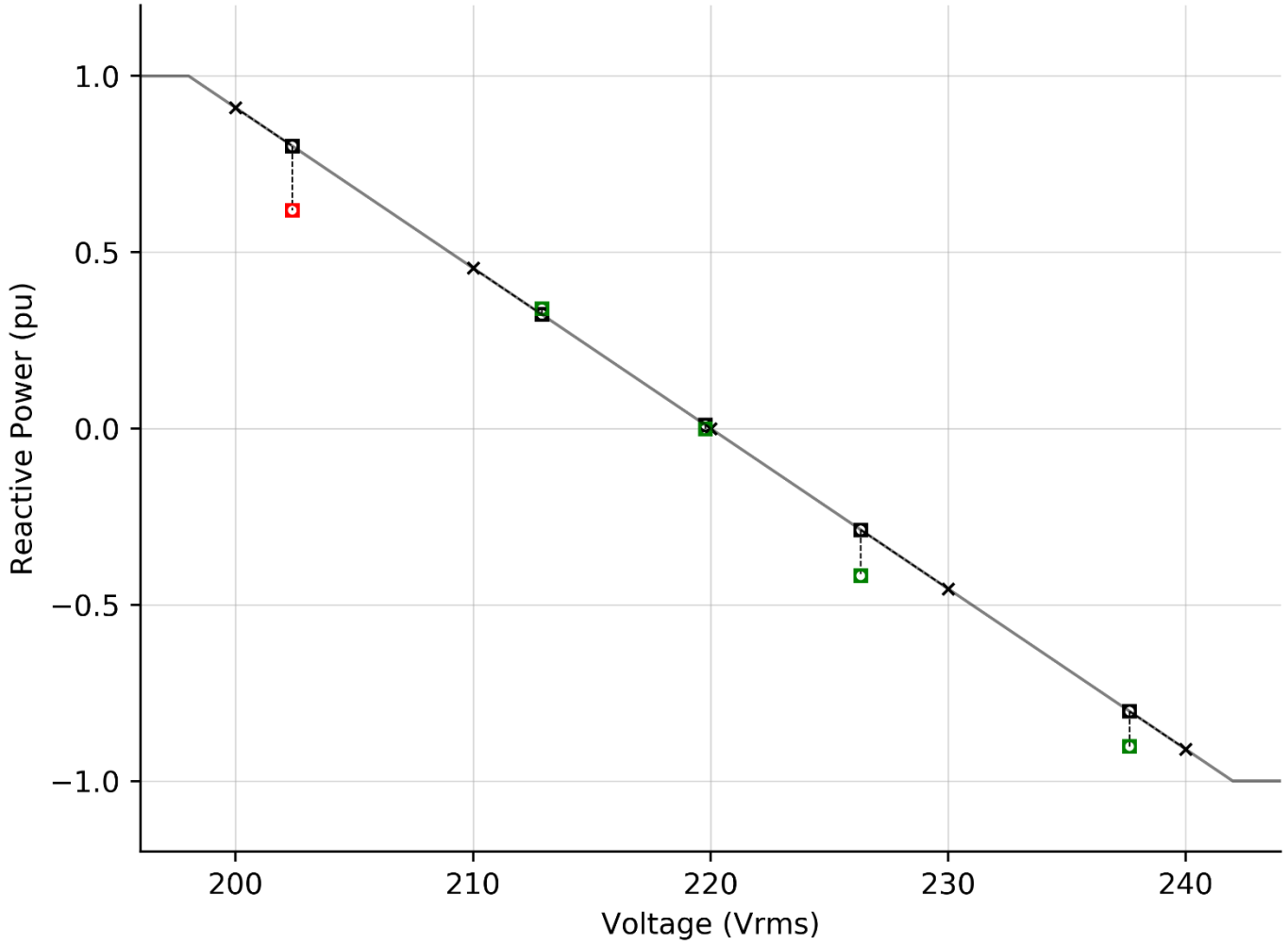
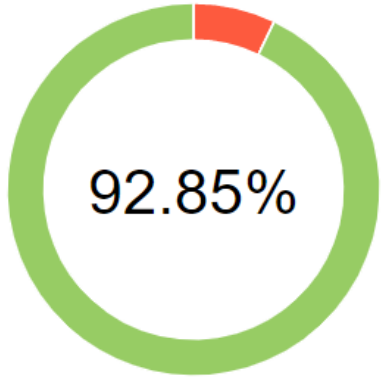
- #2 test_droop[0-58]
- #3 test_droop[0-59]
- #4 test_droop[0-60]
- #5 test_droop[0-61]
- #6 test_droop[0-62]
- #7 test_droop[0-63]

$DER1_{exp}$ $DER1_{avg}Fail$ $DER1_{avg}Ok$ $DER2_{avg}Ok$ Connection

$DER2_{exp}$ $DER2_{avg}Fail$

dVOC





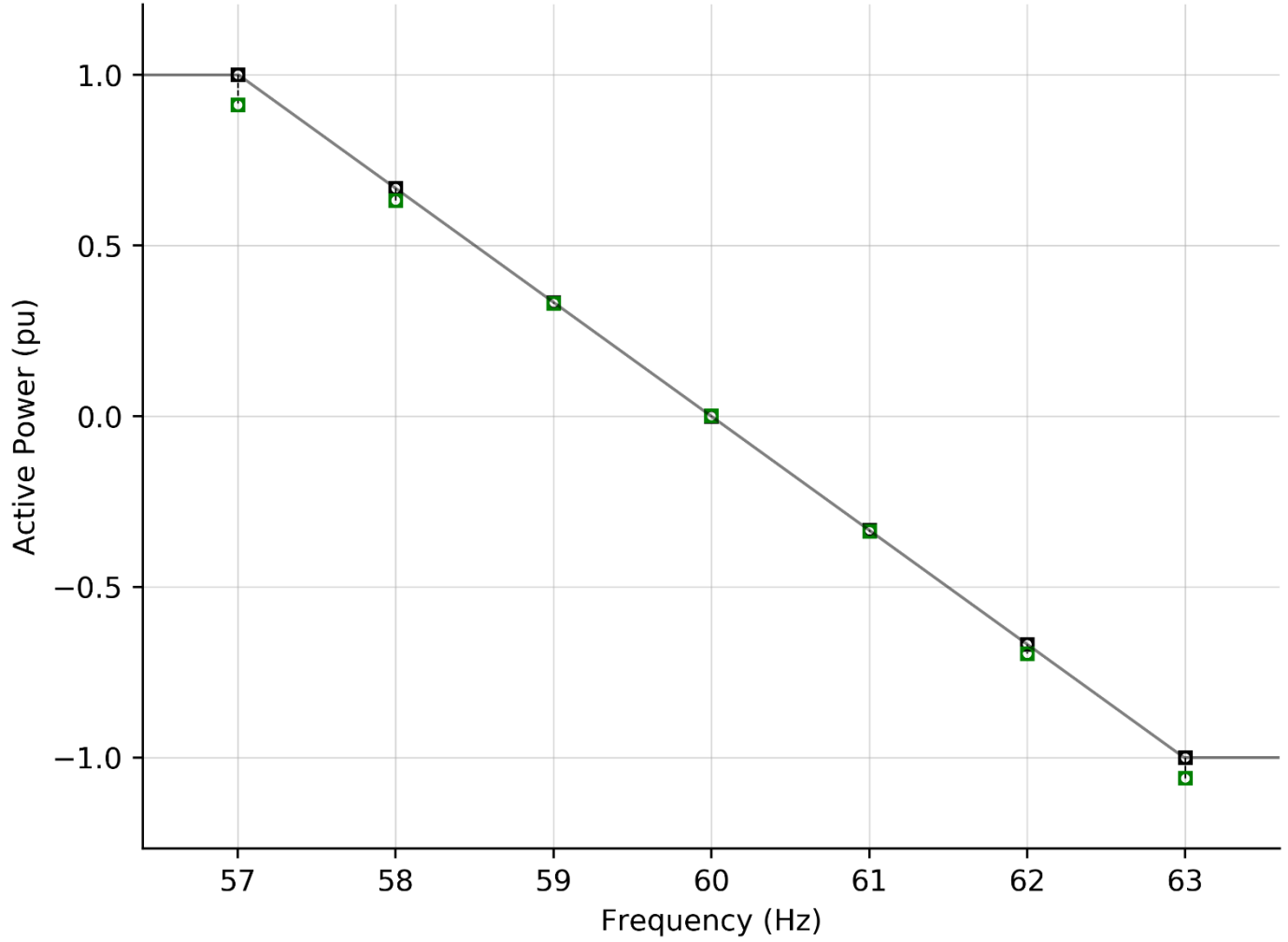
test_02_droop_voltage

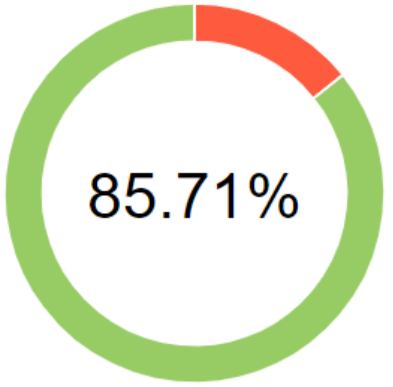
- #1 test_droop[0-200]
- #2 test_droop[0-210]
- #3 test_droop[0-220]
- #4 test_droop[0-230]
- #5 test_droop[0-240]

Org_{exp} $DER2_{exp}$ $DER2_{avg}Fail$ $DER2_{avg}Ok$ Connection

$DER1_{exp}$ $DER1_{avg}Fail$ $DER1_{avg}Ok$

VSG (regulation of Q_{gap})



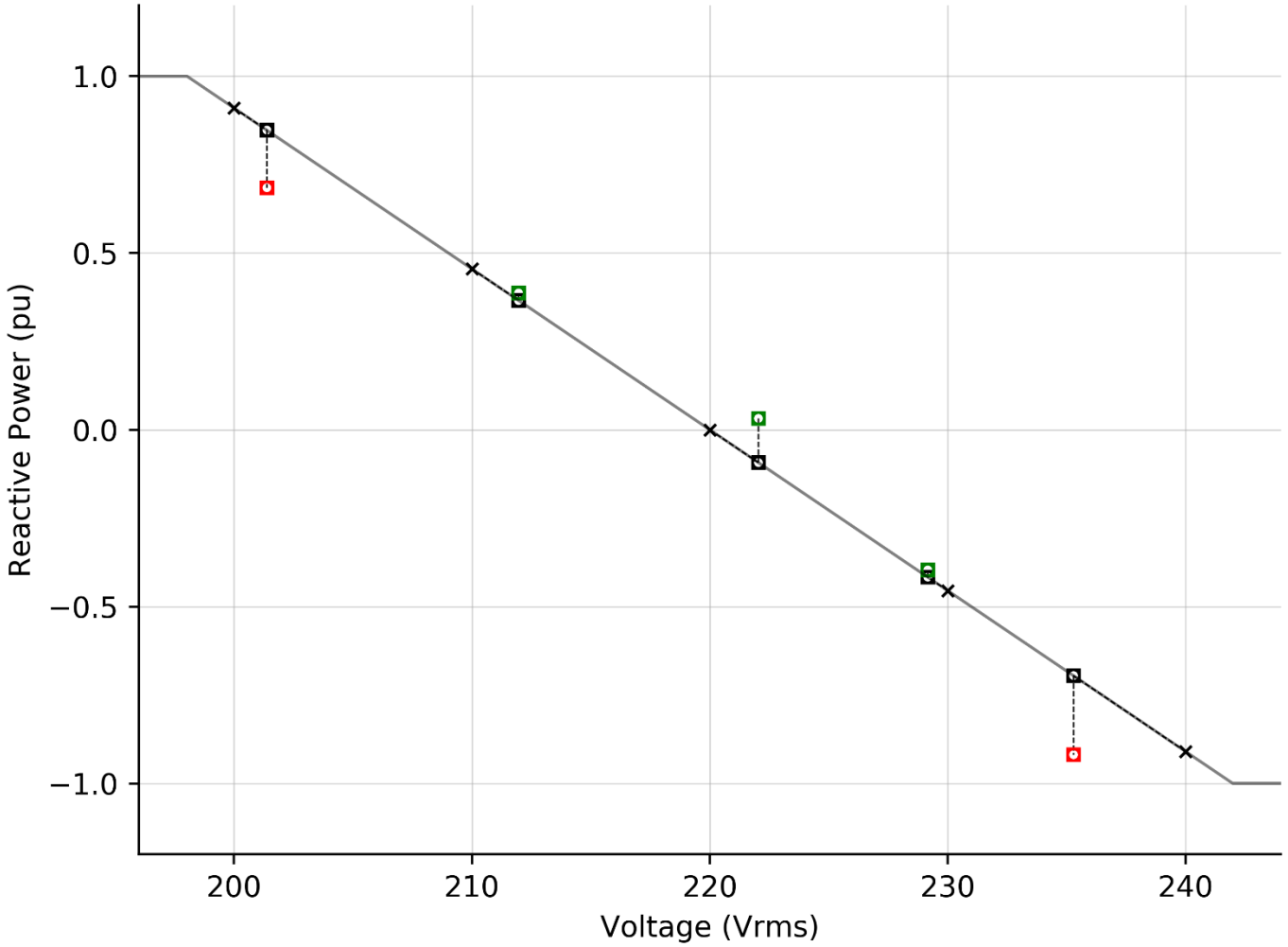


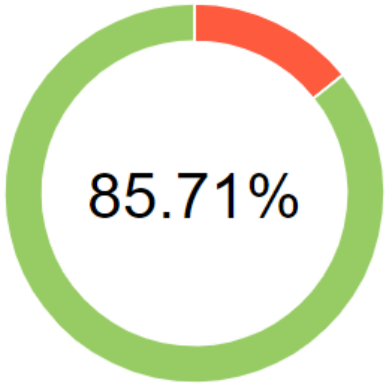
test_01_droop_frequency

- #1 test_droop[0-57]
- #2 test_droop[0-58]
- #3 test_droop[0-59]
- #4 test_droop[0-60]
- #5 test_droop[0-61]
- #6 test_droop[0-62]
- #7 test_droop[0-63]

$DER1_{exp}$ $DER1_{avg}Fail$ $DER1_{avg}Ok$ $DER2_{avg}Ok$ Connection
$DER2_{exp}$ $DER2_{avg}Fail$

VSG (regulation of Q_{gap})





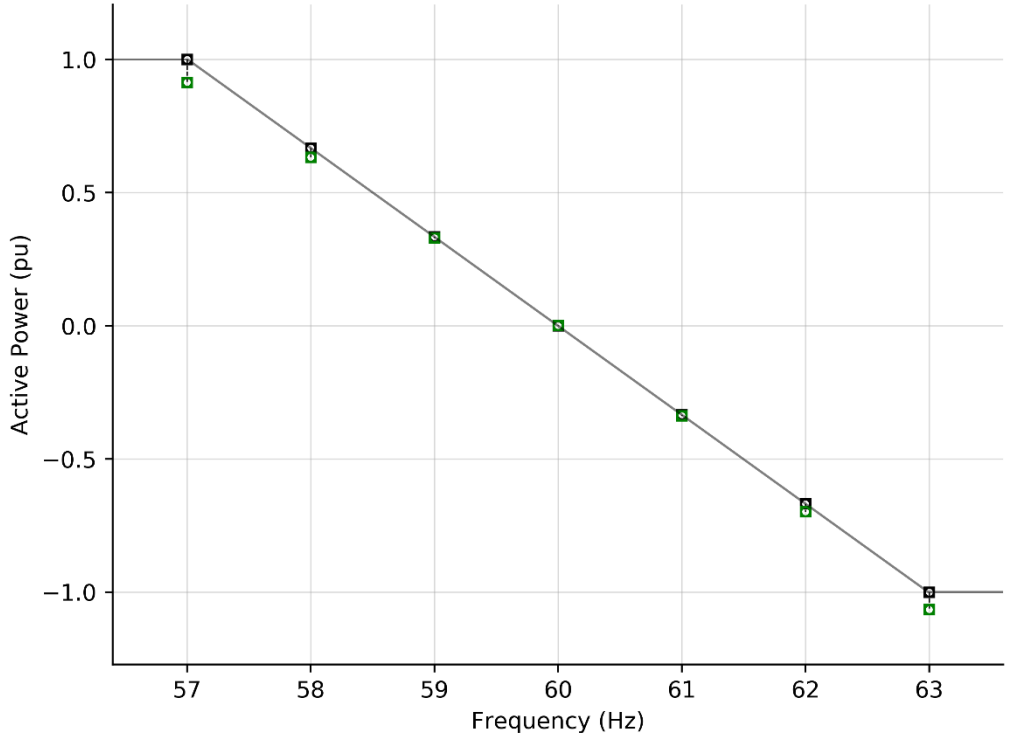
test_02_droop_voltage

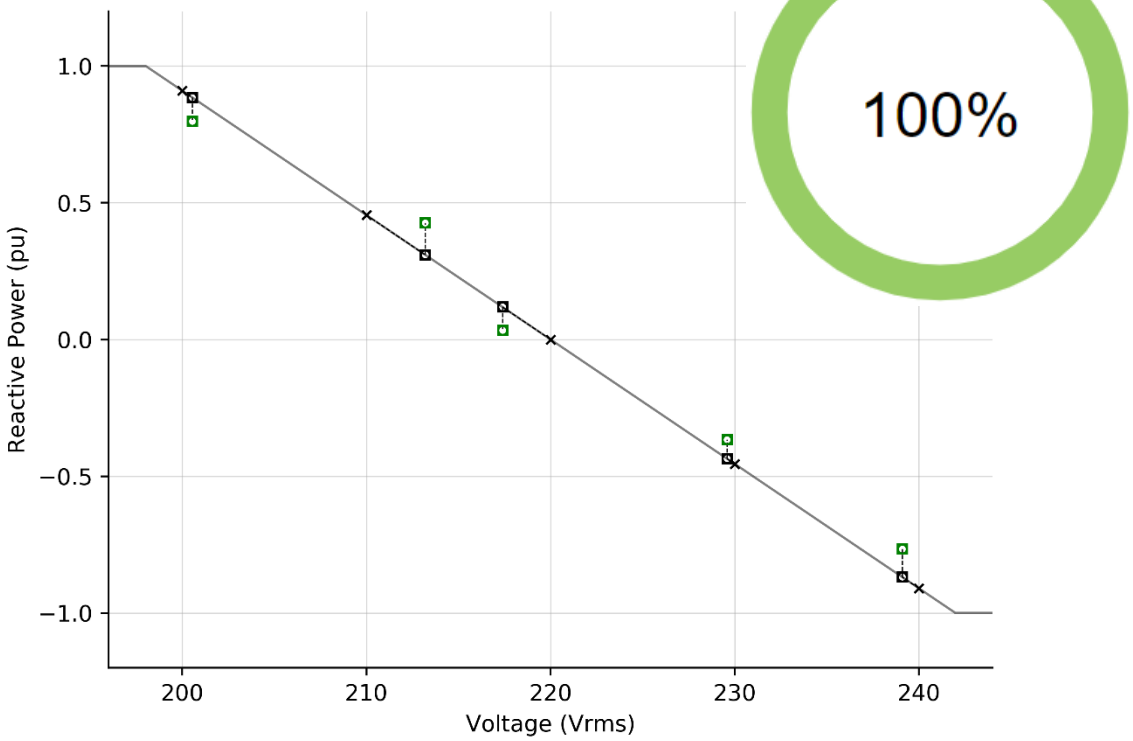
- #1 test_droop[0-200]
- #2 test_droop[0-210]
- #3 test_droop[0-220]
- #4 test_droop[0-230]
- #5 test_droop[0-240]

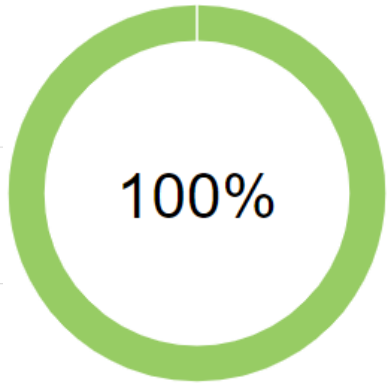
Org_{exp} $DER2_{exp}$ $DER2_{avg}Fail$ $DER2_{avg}Ok$ Connection

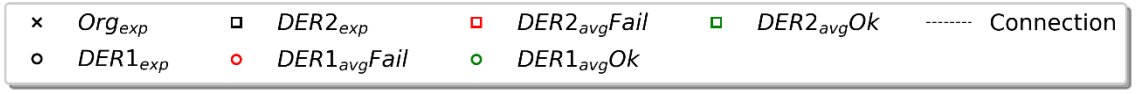
$DER1_{exp}$ $DER1_{avg}Fail$ $DER1_{avg}Ok$

VSG (regulation of Q_{poc})









Summary

- All primary controllers considered passed the frequency support steady-state tests.
- The Droop presented a significant error on the Voltage-Var curve among all other primary controllers considered.
- The VSG with reactive power on the gap failed in the Voltage-Var curve, which has been attributed to the voltage on the virtual inductor.
- Even though the dVOC failed in a point of the Voltage-Var curve, its performance was satisfactory.
- In order to compute the Voltage-Var curves, the voltages are measured at the DER PoC, to avoid the voltage drop in the feeder

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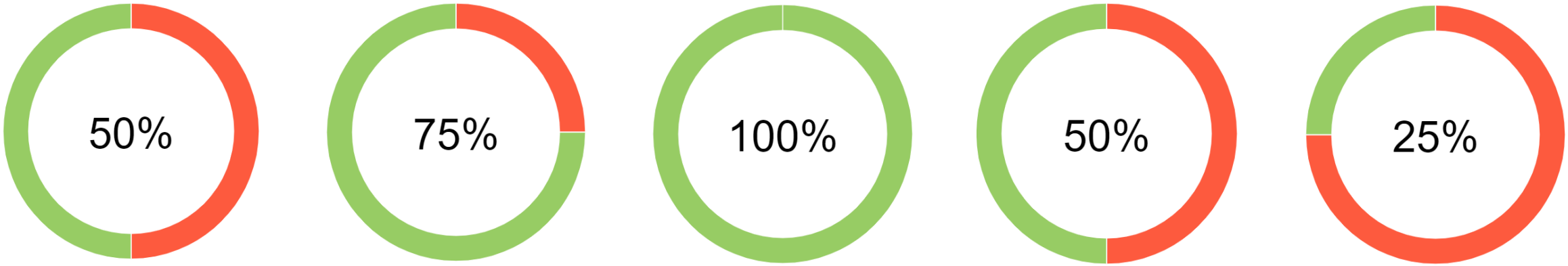
Transition Tests – Unplanned Islanding

Disconnection with

- $P_o = 0$ pu / $Q_o = 0$ pu, with 0% and 70 % of full load
- $P_o = 0.7$ pu / $Q_o = 0.7$ pu, with 0% and 70 % of full load



Droop **2I Droop** **dVOC** **VSG (Q_{gap})** **VSG 2 (Q_{poc})**

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Transition Tests – Unplanned Islanding

Thresholds

```
class ModeTransition:
    # Active power (pu), Reactive power (pu), R1 Load, R2 Load
    condition = [(0, 0, False, False),
                 (0.7, 0.7, False, False),
                 (0, 0, True, True),
                 (0.7, 0.7, True, True),
                 ]

    time_before_change = 0.5  # s (Time before the event)
    time_after_change = 1.5  # s (Time after the start of the event)

    voltage_sag = False  # create a voltage sag before disconnecting?

    # Thresholds:
    max_voltage_rms_os = 30  # V (Maximum voltage after disconnecting from the grid)
    max_voltage_rms_st = 1  # s (Maximum Vrms settling time. Settling time region = +/-5Vrms of last value in capture)
    max_voltage_freq_st = 1  # s (Maximum Frequency settling time. Settling time region = +/-0.01 of last value in captur
    max_voltage_rms_ss_error = 20  # V (Maximum Vrms steady state error compared with nominal value, after transition)
    max_frequency_error = 3  # Hz (Maximum frequency steady state error compared with nominal value, after transition)
```

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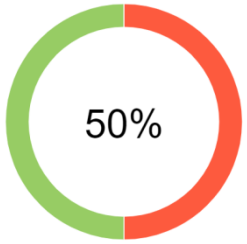
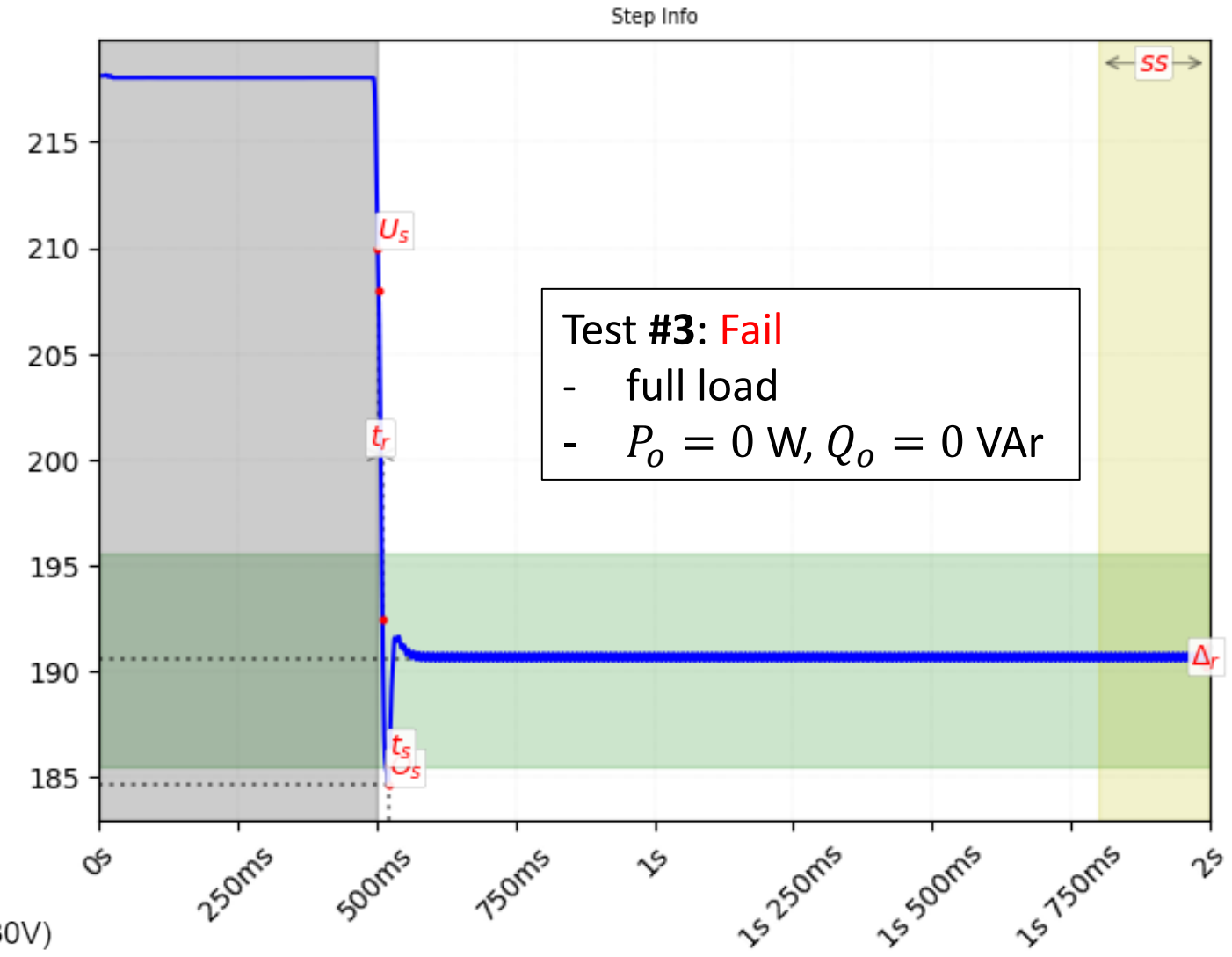
Droop control

Test Suite

test_disconnection

- #1 test_grid_disconnection[0-0-False-False]
- #3 test_grid_disconnection[0-0-True-True]
- #2 test_grid_disconnection[0.7-0.7-False-False]
- #4 test_grid_disconnection[0.7-0.7-True-True]





Test **#3**: Fail
- full load
- $P_o = 0$ W, $Q_o = 0$ VAr

Test body

- PASS -> DER2: Overshoot = -5.879070877642789V (max = 30V)
- FAIL -> DER1: Vrms error = 29.345235342517952V (max = 20V)
- FAIL -> DER2: Vrms error = 29.345270441626326V (max = 20V)
- PASS -> DER1: Settling time = 0.020599999s (max = 1s)

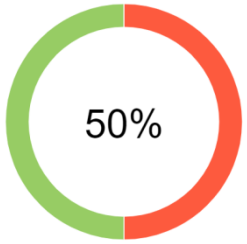
Same error for both DERs

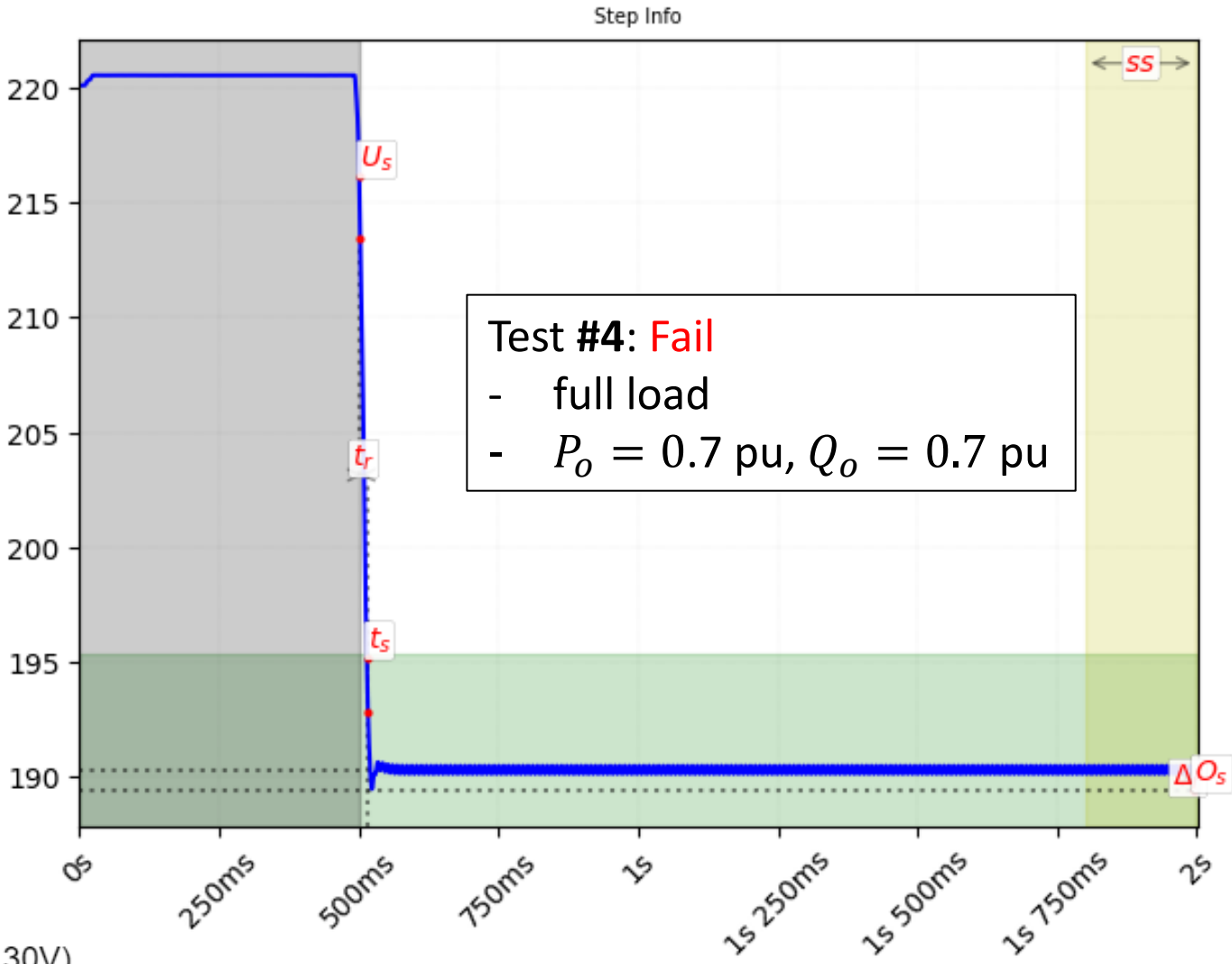
Droop control

Test Suite

test_disconnection

- #1 test_grid_disconnection[0-0-False-False]
- #3 test_grid_disconnection[0-0-True-True]
- #2 test_grid_disconnection[0.7-0.7-False-False]
- #4 test_grid_disconnection[0.7-0.7-True-True]





Test **#4**: Fail
- full load
- $P_o = 0.7$ pu, $Q_o = 0.7$ pu

Test body

- PASS -> DER2: Overshoot = -0.8990097993671782V (max = 30V)
- FAIL -> DER1: Vrms error = 29.72293182137352V (max = 20V)
- FAIL -> DER2: Vrms error = 29.722926036672675V (max = 20V)
- PASS -> DER1: Settling time = 0.0136s (max = 1s)

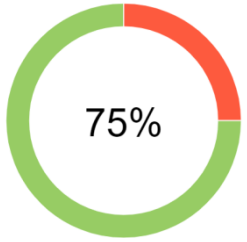
} Same error for both DERs

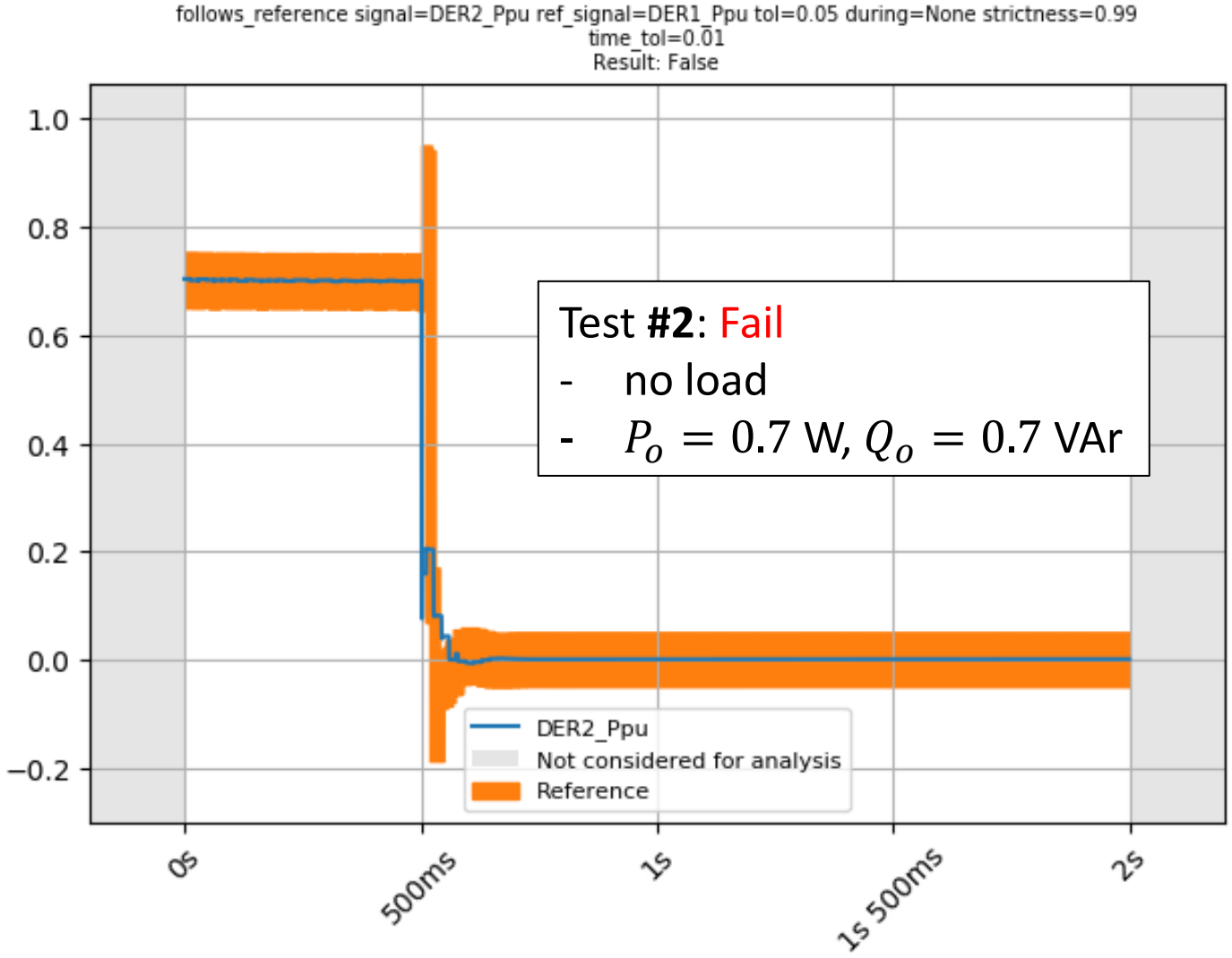
2I-Droop control

Test Suite

test_disconnection

- #1 test_grid_disconnection[0-0-False-False]
- #3 test_grid_disconnection[0-0-True-True]
- #2 test_grid_disconnection[0.7-0.7-False-False]
- #4 test_grid_disconnection[0.7-0.7-True-True]





Test body

FAIL -> DER Active power tracking (among the DERs)

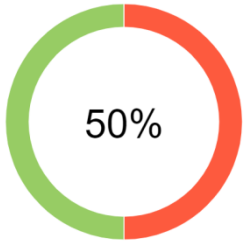
No power sharing soon after the disconnection

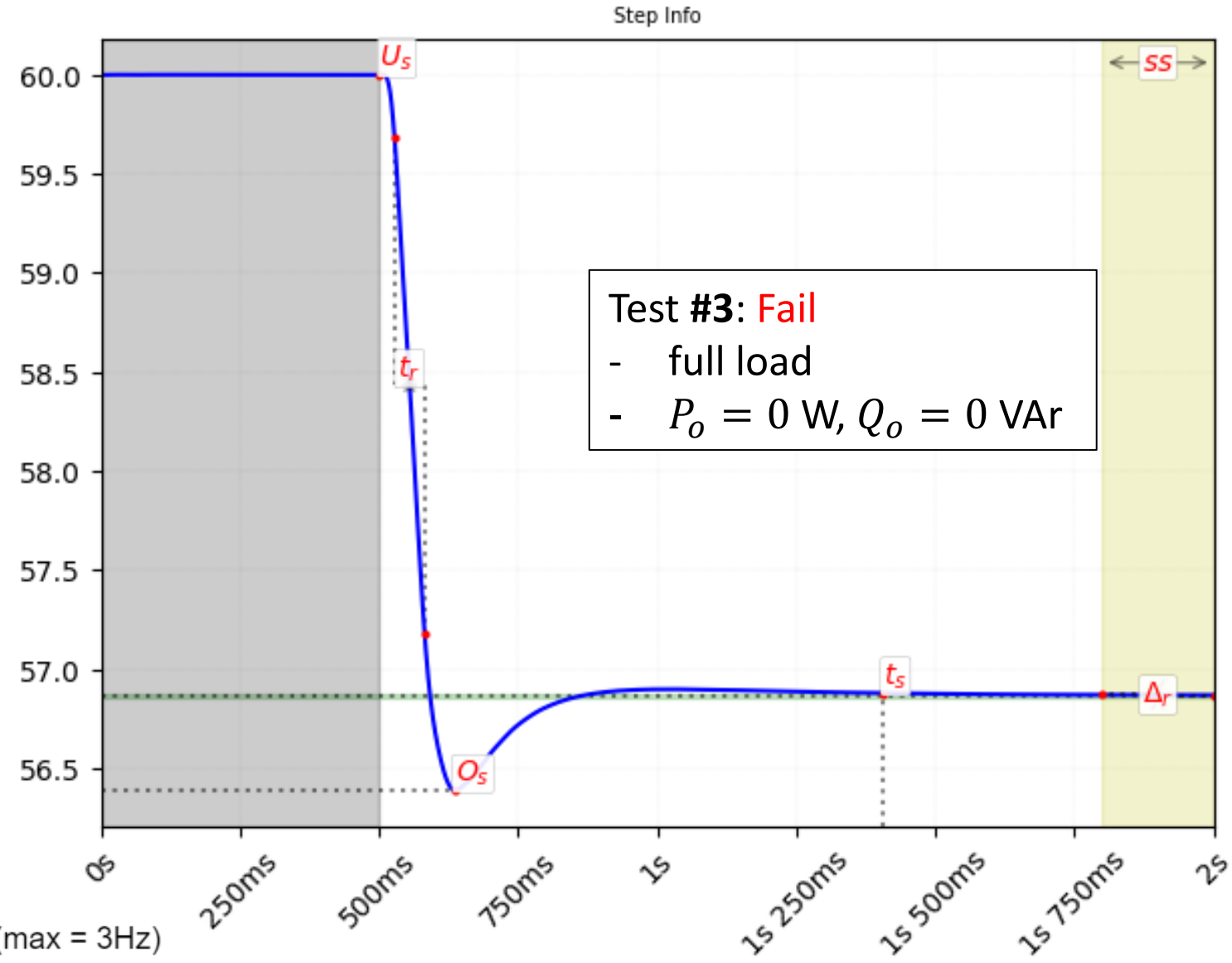
VSG (regulation of Q_{gap})

Test Suite

test_disconnection

- #1 test_grid_disconnection[0-0-False-False]
- #3 test_grid_disconnection[0-0-True-True]
- #2 test_grid_disconnection[0.7-0.7-False-False]
- #4 test_grid_disconnection[0.7-0.7-True-True]





Test **#3**: Fail
- full load
- $P_o = 0$ W, $Q_o = 0$ VAr

Test body

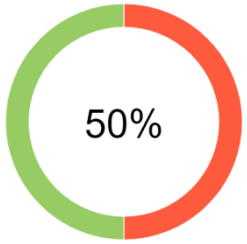
FAIL -> Frequency error = 3.1290245056152344Hz (max = 3Hz)

VSG (regulation of Q_{gap})

Test Suite

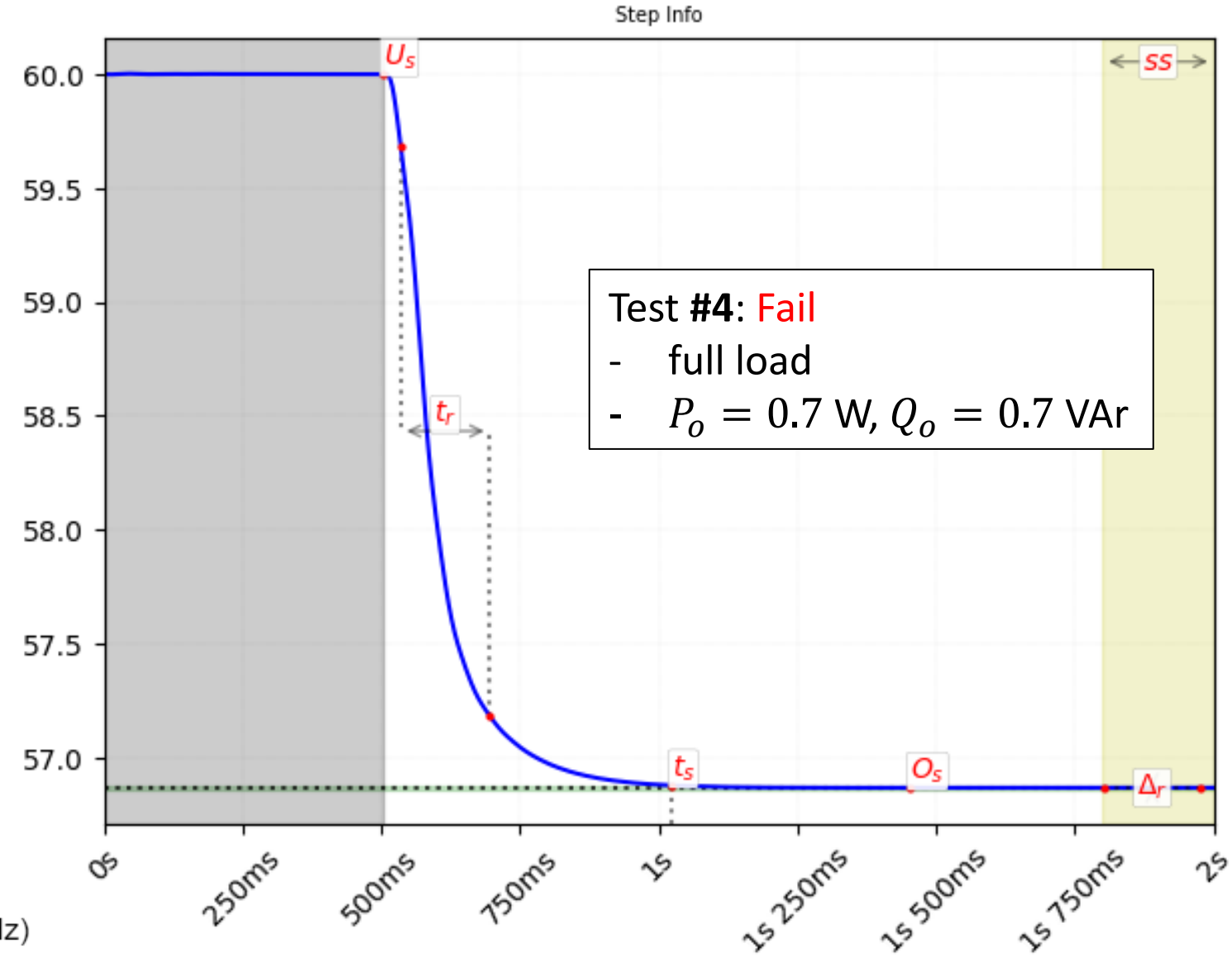
test_disconnection

- #1 test_grid_disconnection[0-0-False-False]
- #3 test_grid_disconnection[0-0-True-True]
- #2 test_grid_disconnection[0.7-0.7-False-False]
- #4 test_grid_disconnection[0.7-0.7-True-True]



Test body

FAIL -> Frequency error = 3.130859375Hz (max = 3Hz)



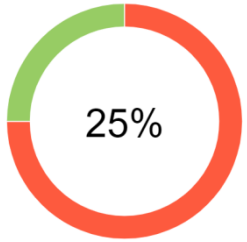
Test **#4**: Fail
- full load
- $P_o = 0.7$ W, $Q_o = 0.7$ VAr

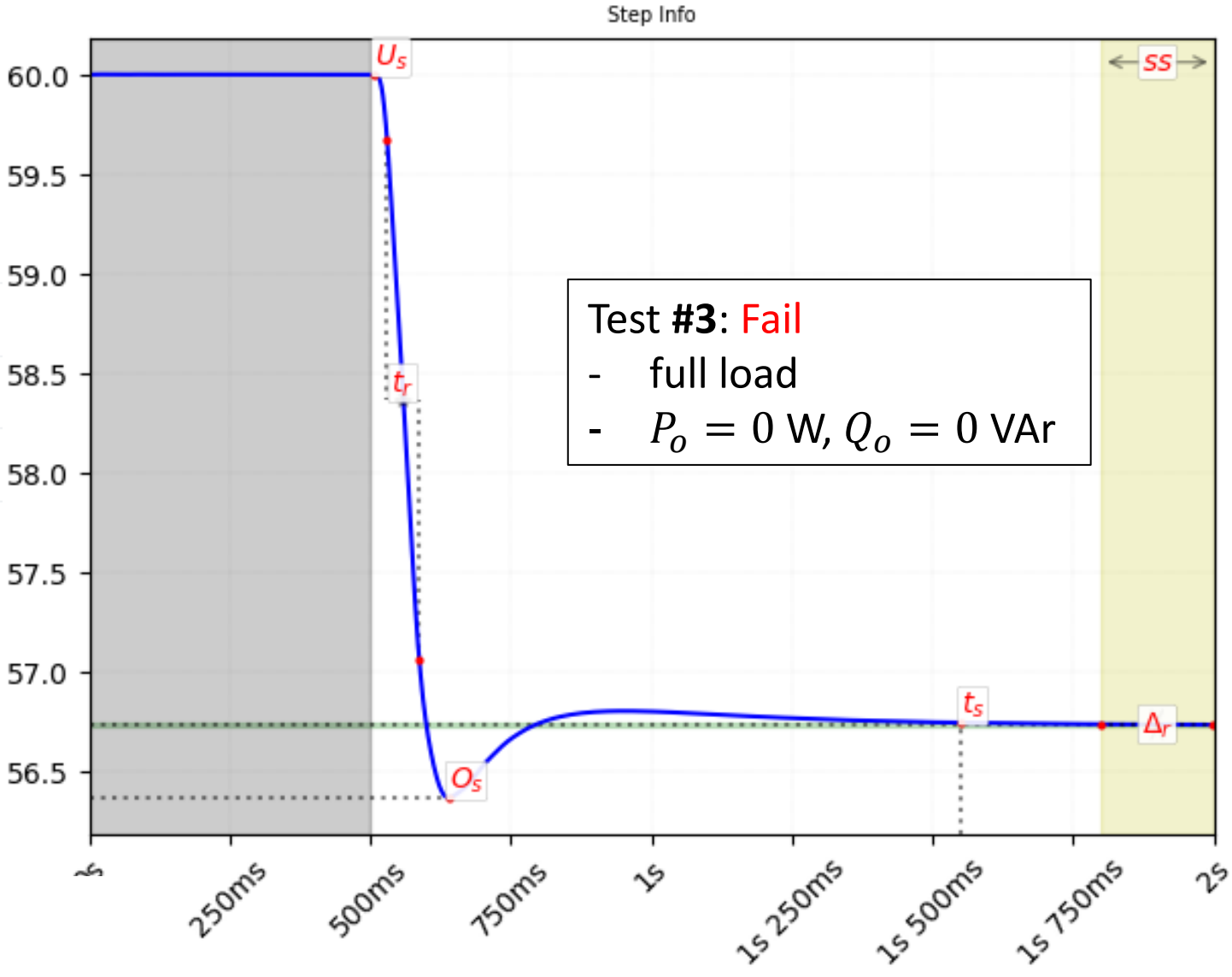
VSG (regulation of Q_{poc})

Test Suite

test_disconnection

- #1 test_grid_disconnection[0-0-False-False]
- #3 test_grid_disconnection[0-0-True-True]
- #2 test_grid_disconnection[0.7-0.7-False-False]
- #4 test_grid_disconnection[0.7-0.7-True-True]





Test **#3**: Fail
- full load
- $P_o = 0$ W, $Q_o = 0$ VAr

Test body

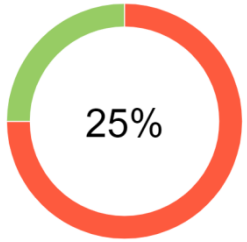
- PASS -> DER1: Settling time = 0.3031s (max = 1s)
- PASS -> DER2: Settling time = 0.3031s (max = 1s)
- FAIL -> Freq: Settling time = 1.0487s (max = 1s)
- FAIL -> Frequency error = 3.2662086486816406Hz (max = 3Hz)

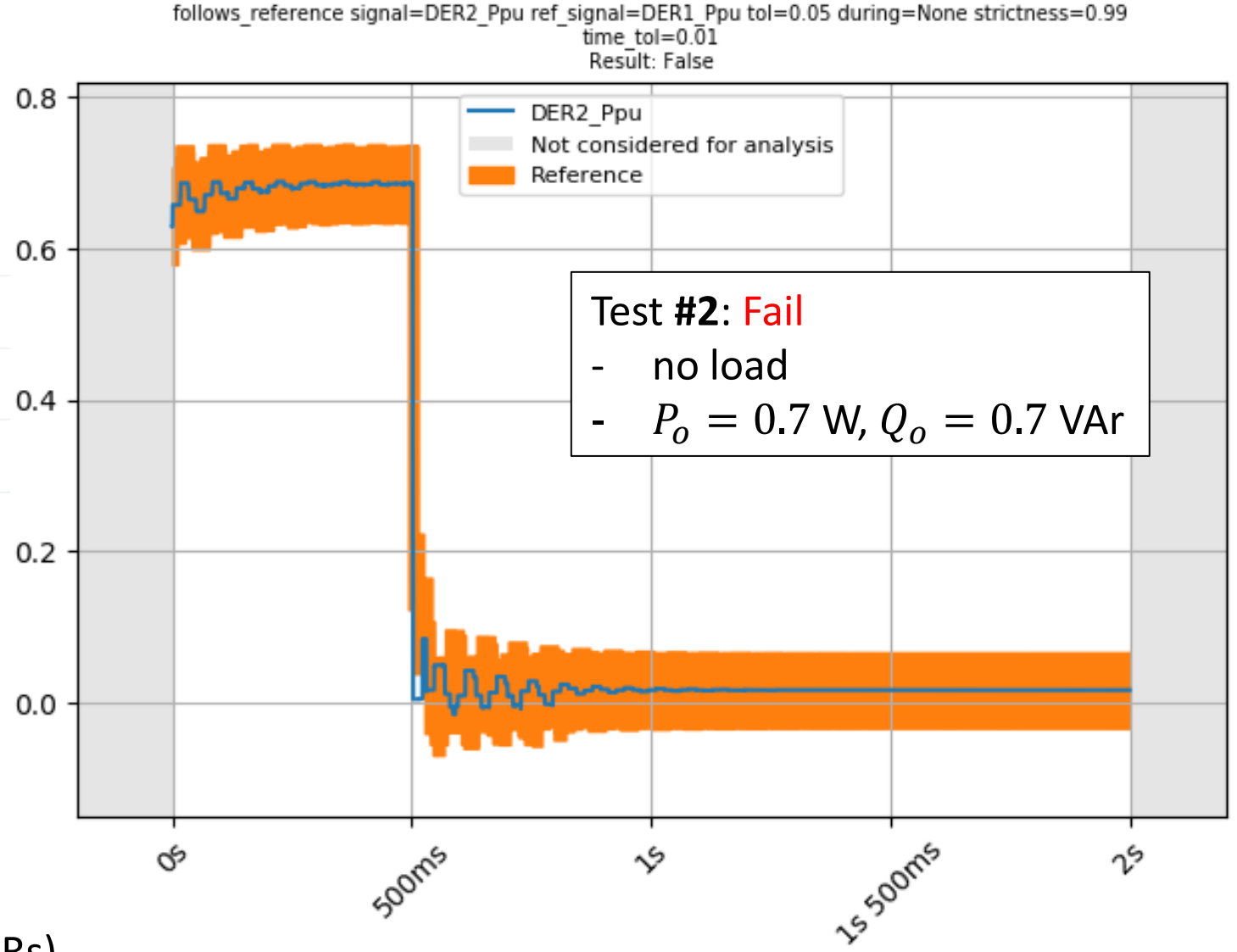
VSG (regulation of Q_{poc})

Test Suite

test_disconnection

- #1 test_grid_disconnection[0-0-False-False]
- #3 test_grid_disconnection[0-0-True-True]
- #2 test_grid_disconnection[0.7-0.7-False-False]
- #4 test_grid_disconnection[0.7-0.7-True-True]





Test body

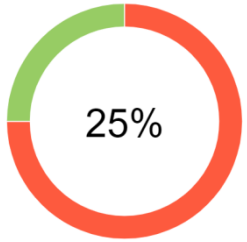
FAIL -> DER Active power tracking (among the DERs)

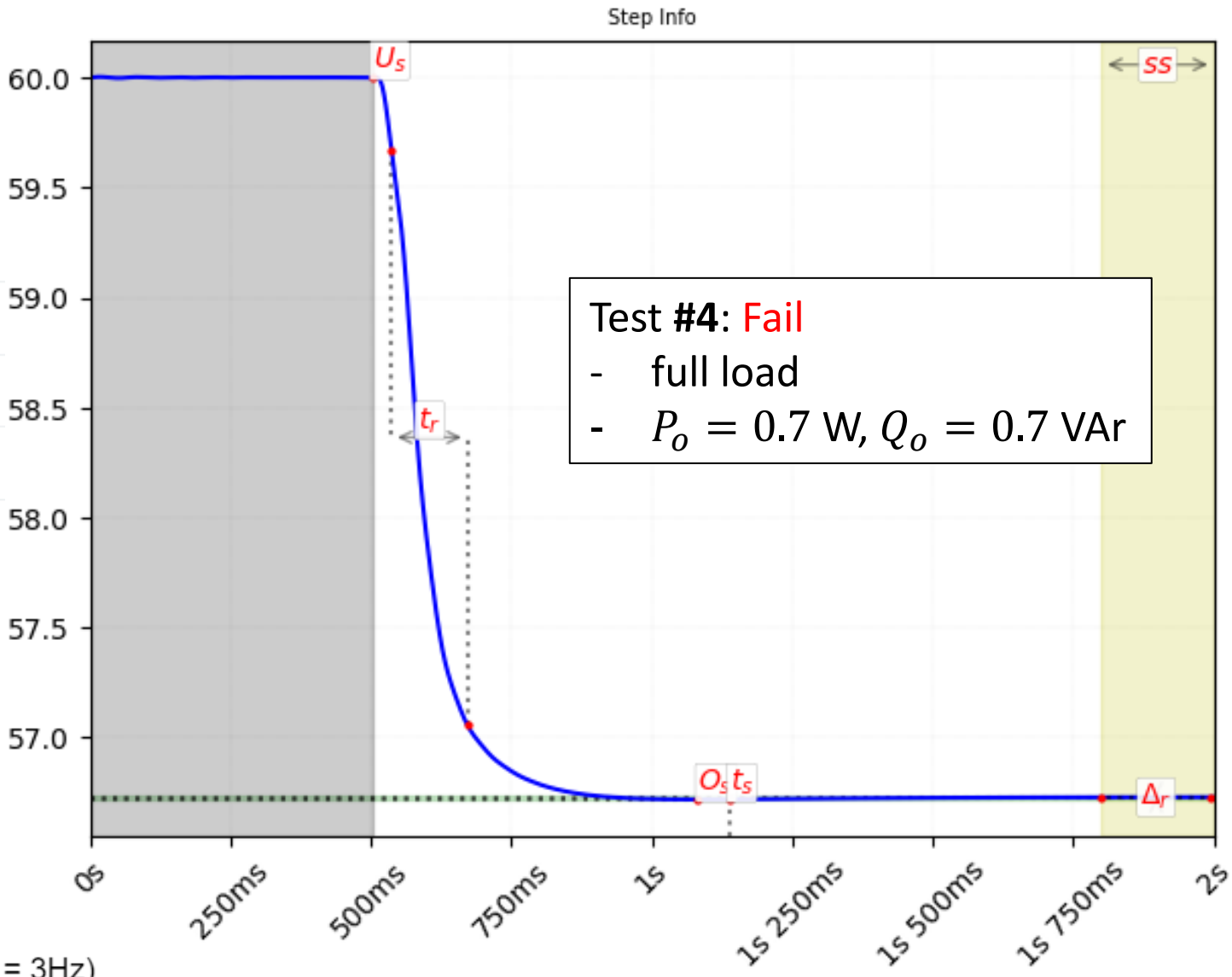
VSG (regulation of Q_{poc})

Test Suite

test_disconnection

- #1 test_grid_disconnection[0-0-False-False]
- #3 test_grid_disconnection[0-0-True-True]
- #2 test_grid_disconnection[0.7-0.7-False-False]
- #4 test_grid_disconnection[0.7-0.7-True-True]





Test **#4**: Fail
- full load
- $P_o = 0.7$ W, $Q_o = 0.7$ VAr

Test body

FAIL -> Frequency error = 3.2705535888671875Hz (max = 3Hz)

Summary

Let us summarize the results from the unplanned islanding test.

The automated test points out that the dVOC presented the best results.

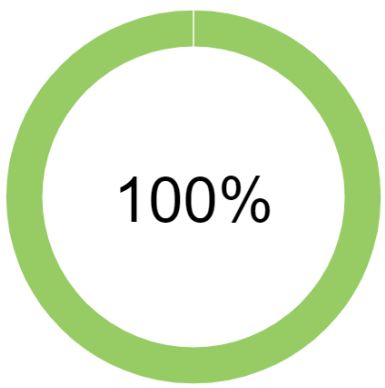
A detailed analysis reveals that 2I-Droop and the VSGs with adjustment in the control parameters could also good results meeting the defined requirements.

The communication delay between the MGCC and the DERs could change the results of this test.

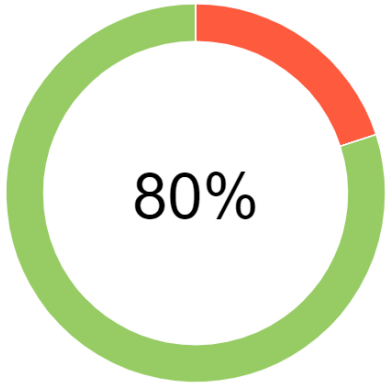
Islanding Mode Tests

Performed tests:

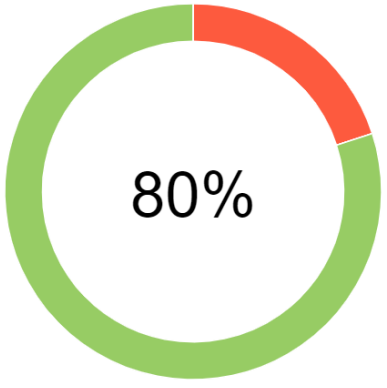
- ❑ Linear load (33 % and 66% of full load)
- ❑ Nonlinear load (50 % of full load)
- ❑ Short-circuit (at $t = 0.05$ sec and at $t = 0.25$ sec)



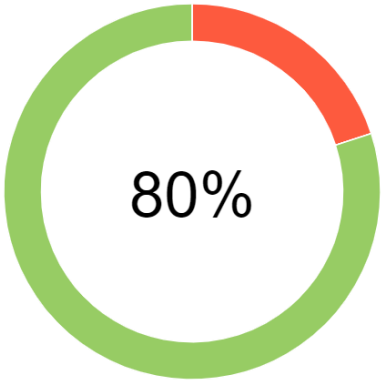
Droop



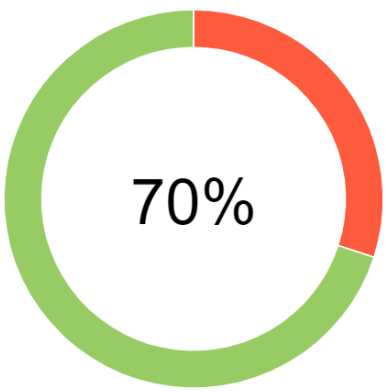
2I Droop



dVOC



VSG (Q_{gap})



VSG 2 (Q_{poc})

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Islanding Mode Tests - Thresholds

```python
class Linear:
    time_before_change = 0.1  # s (Time before the event)
    time_after_change = 0.3  # s (Time after the start of the event)

    # Thresholds:
    max_voltage_rms_os = 22  # V (Maximum voltage after changing the load)
    max_voltage_rms_st = 0.5  # s (Maximum Vrms settling time. Settling time region = +/-5Vrms of last value in capture)
    max_voltage_rms_ss_error = 35  # V (Maximum Vrms steady state error compared with nominal value, after load transition)
    max_frequency_error = 3  # Hz (Maximum frequency steady state error compared with nominal value, after load transition)
```

```python
class NonLinear:
    time_before_change = 0.2  # s (Time before the event)
    time_after_change = 0.5  # s (Time after the start of the event)

    # Thresholds:
    max_voltage = 357  # V (Maximum voltage after removing the load)
    max_current = 400  # A (Maximum peak current during load)
    max_voltage_rms_os = 100  # V (Maximum Vrms overshoot during load)
    max_voltage_rms_st = 0.5  # s (Maximum Vrms settling time. Settling time region = +/-5Vrms of last value in capture)
    max_voltage_rms_ss_error = 20  # V (Maximum Vrms steady state error compared with nominal value, until load is removed)
    max_frequency_error = 1.5  # Hz (Maximum frequency steady state error compared with nominal value, until load is removed)
```

```python
class Short:
    short_duration_range = [0.05, 0.25]  # s (Short circuit duration test points)

    time_before_change = 0.2  # s (Time before the event)
    time_after_change = 0.5  # s (Time after the start of the event)

    # Thresholds:
    max_voltage = 800  # V (Maximum voltage after returning from the short condition)
    max_current = 400  # A (Maximum peak current during short)
    max_voltage_rms_os = 300  # V (Maximum Vrms overshoot)
    max_voltage_rms_st = 0.5  # s (Maximum Vrms settling time. Settling time region = +/-5Vrms of last value in capture)
    max_voltage_rms_ss_error = 100  # V (Maximum steady state error compared with nominal value, after the short event)
    max_frequency_error = 5  # Hz (Maximum frequency error after the short event)
```

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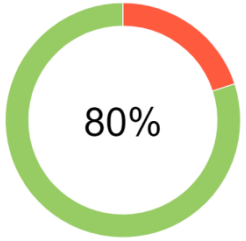
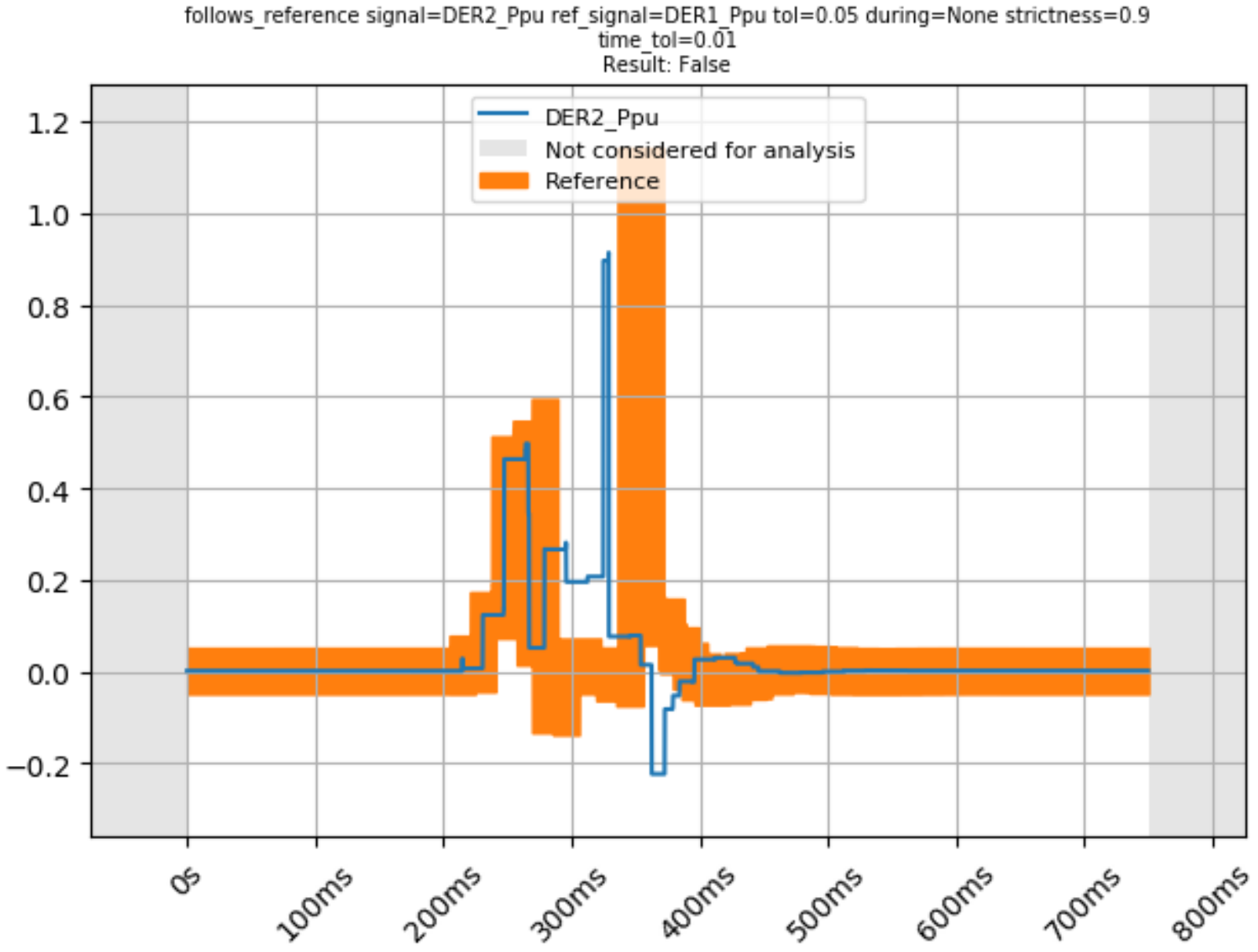
2I-Droop control

Test Suite



- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]

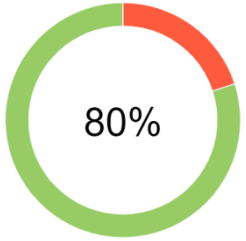


Test body

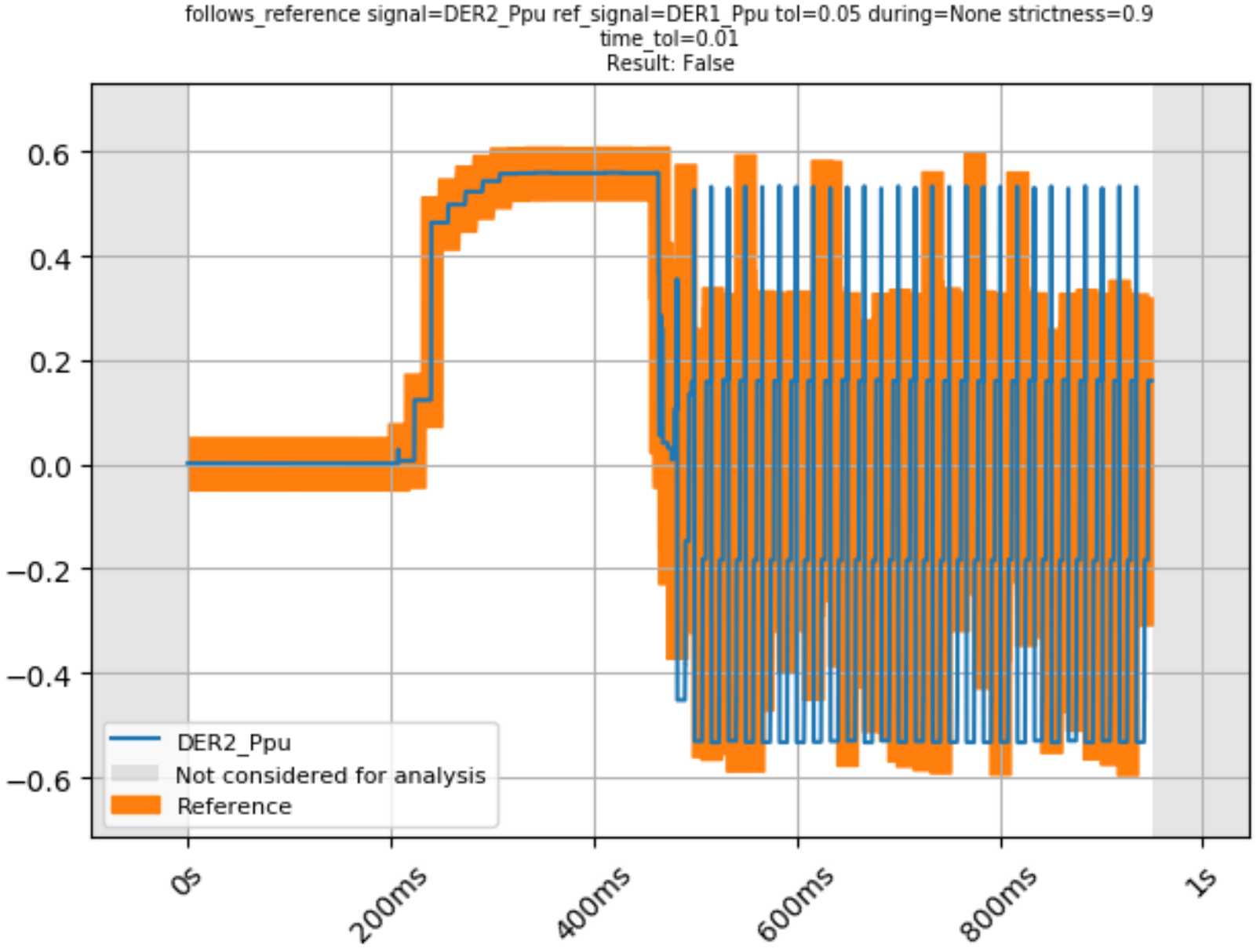
FAIL -> DER Active power tracking (among the DERs)

2I-Droop control

Test Suite



- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]

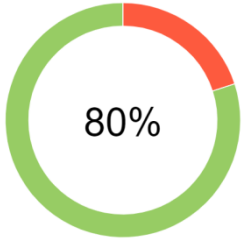


Test body

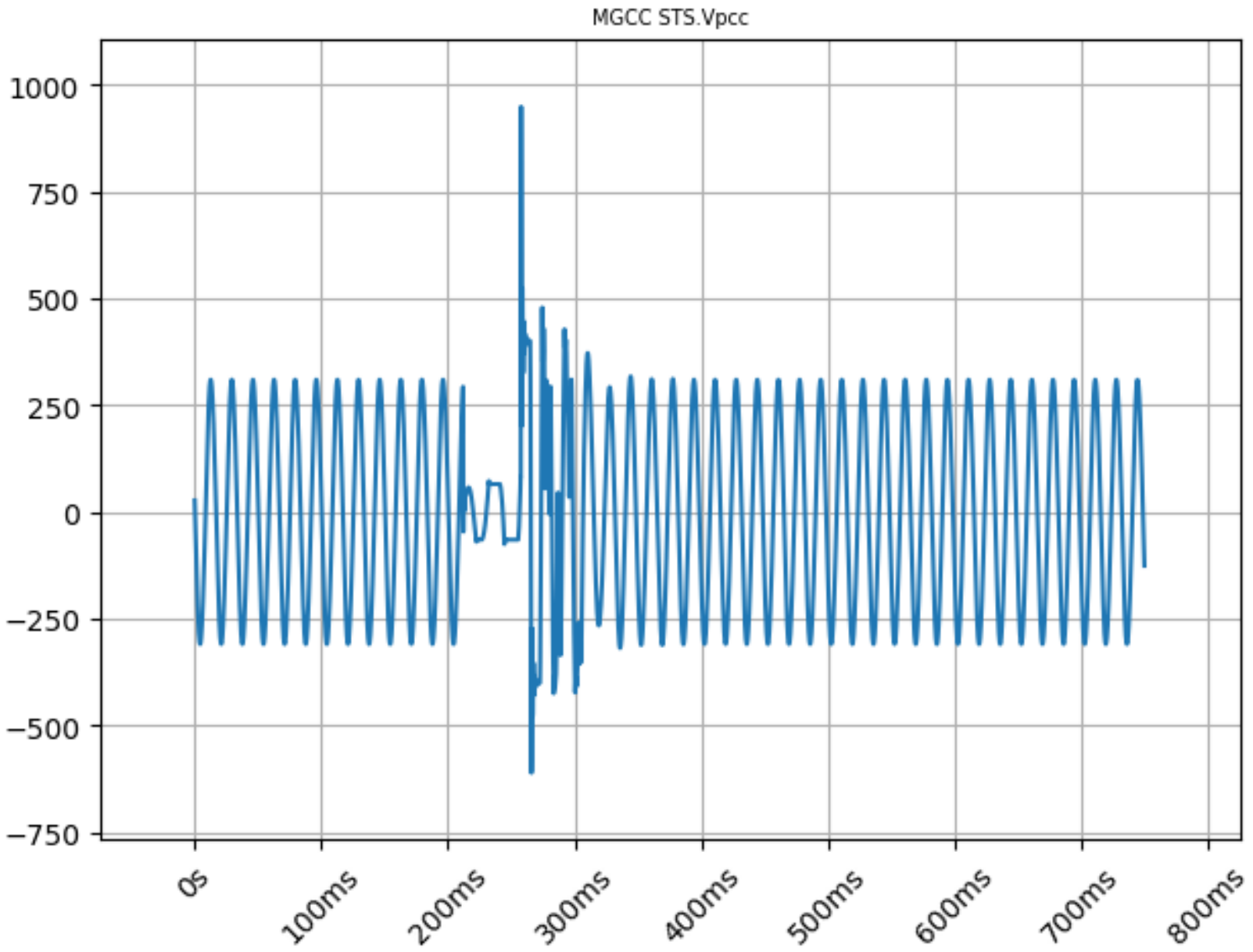
FAIL -> DER Active power tracking (among the DERs)

dVOC

Test Suite



- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]

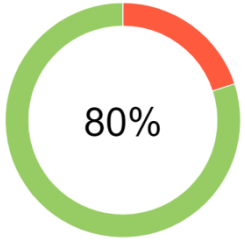


Test body

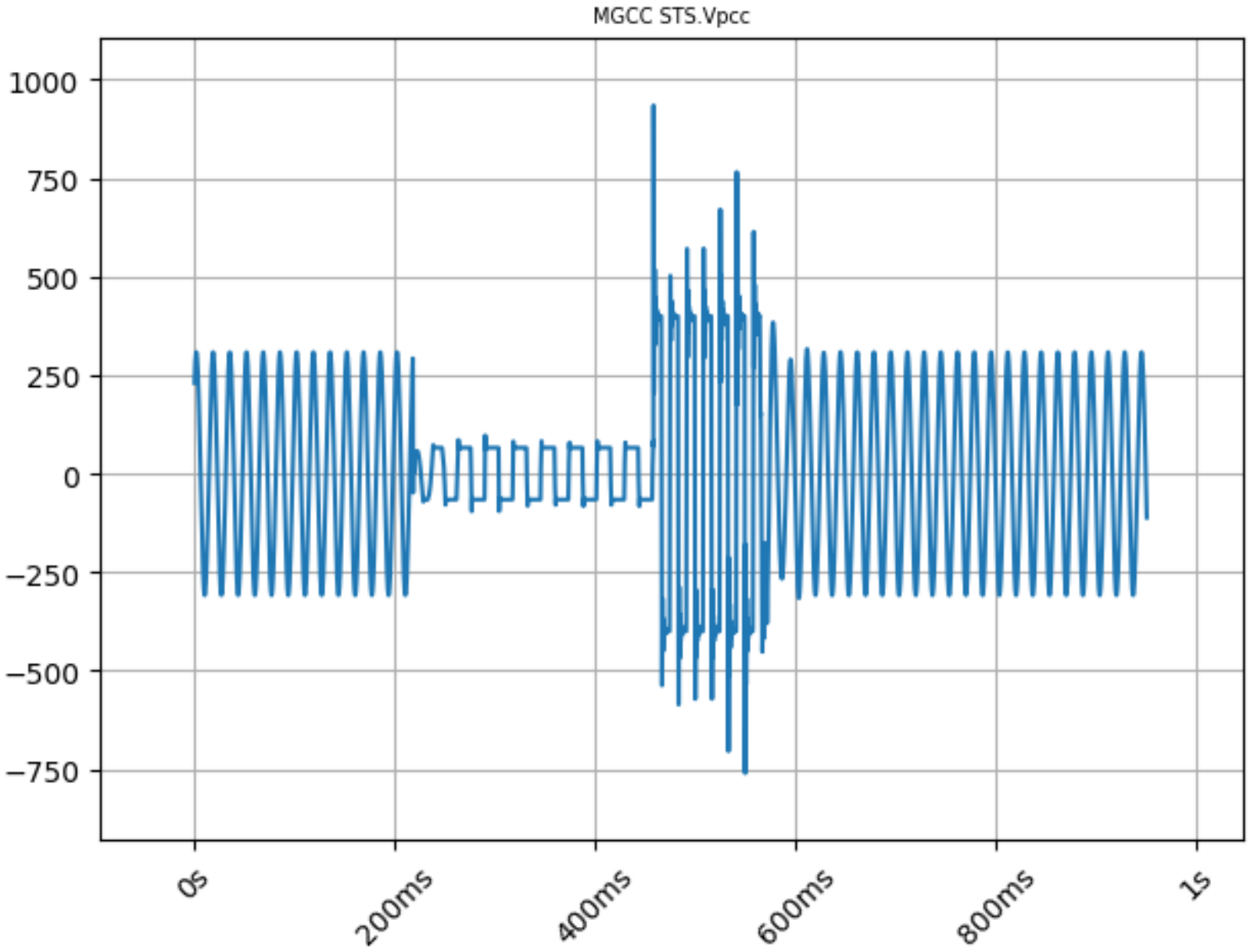
FAIL -> Vmax = 948.0486450195312V (max = 800V) (at the PCC)

dVOC

Test Suite



- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]



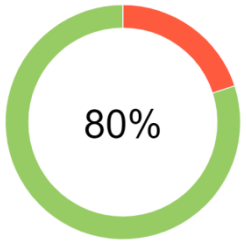
Test body

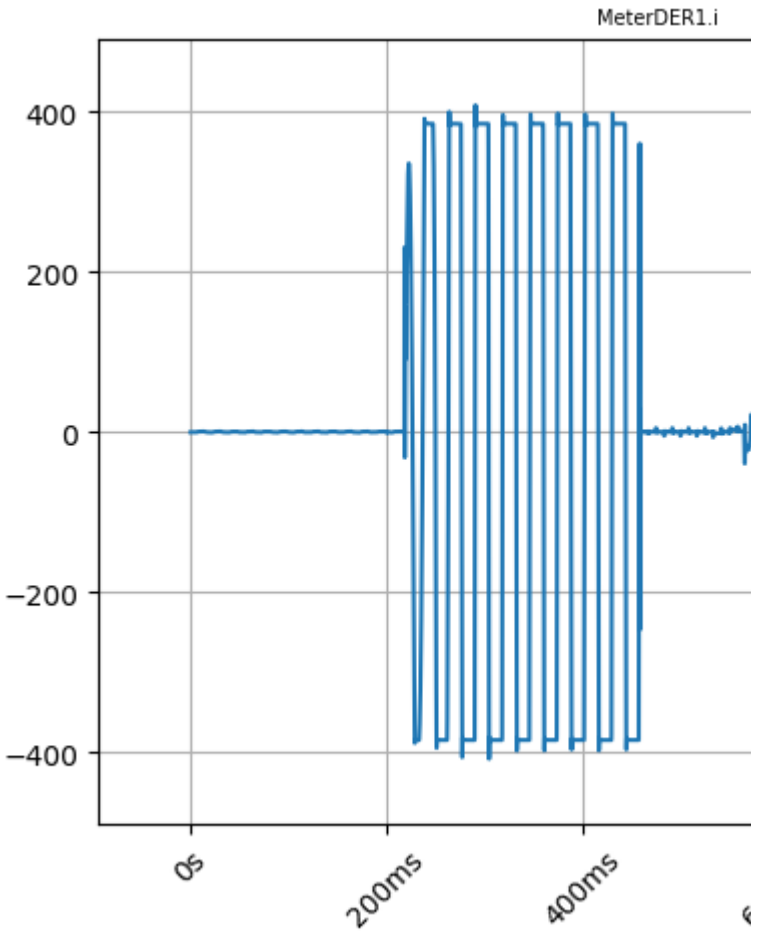
FAIL -> Vmax = 934.875732421875V (max = 800V) (at the PCC)

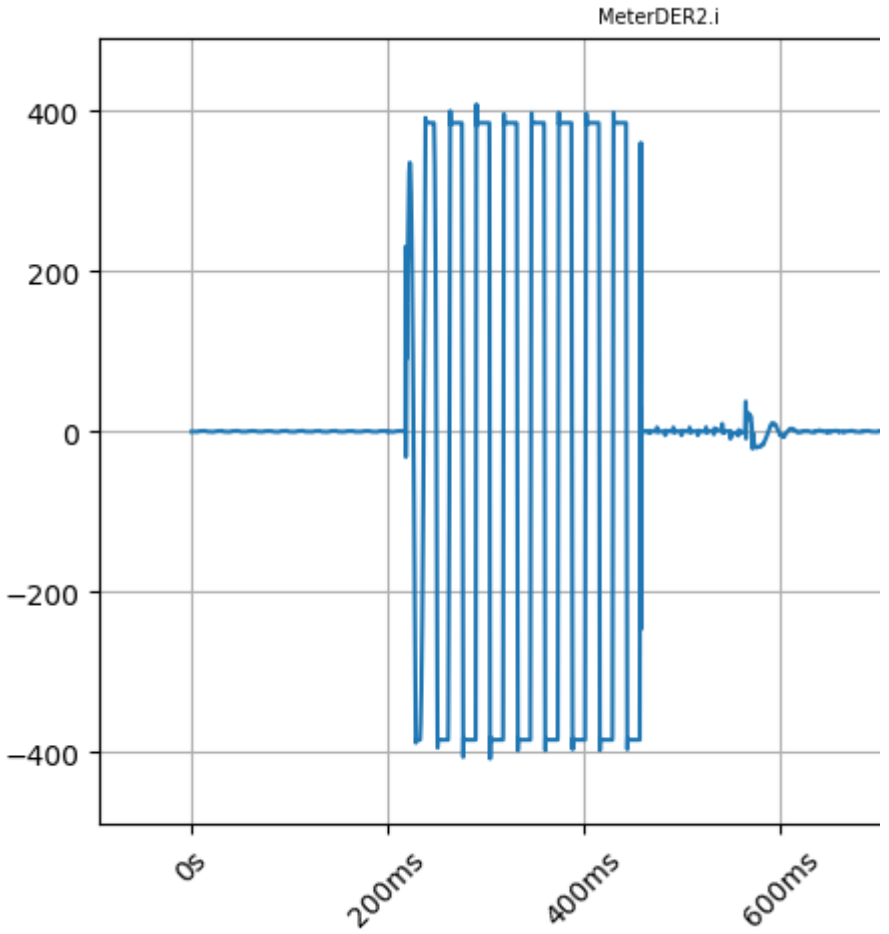
dVOC

Test Suite

- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]

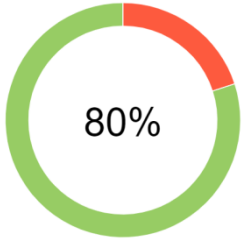




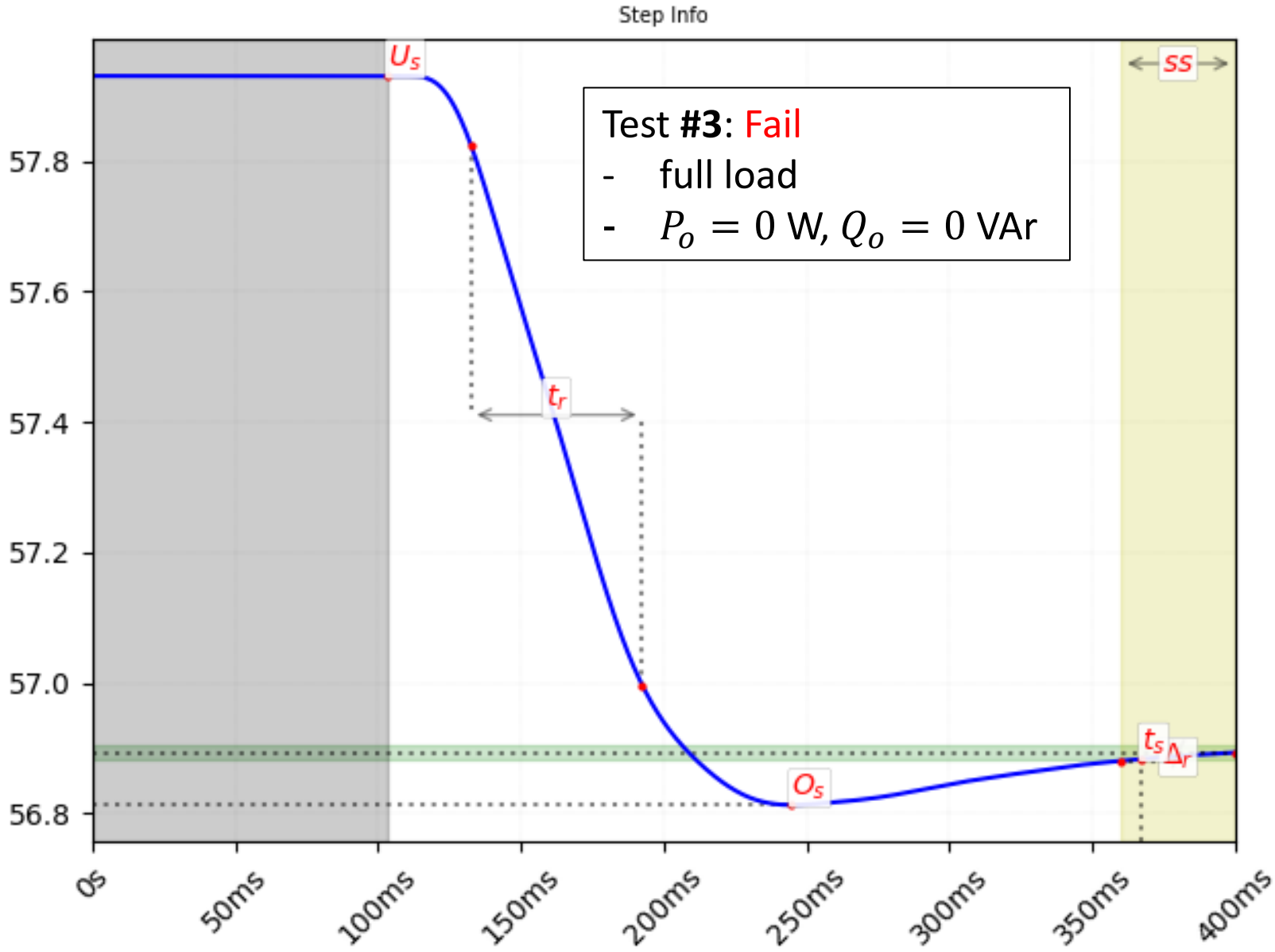


VSG (regulation of Q_{gap})

Test Suite



- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]



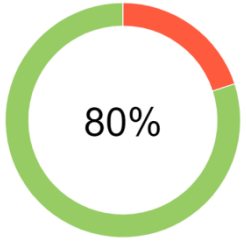
Test **#3**: Fail
- full load
- $P_o = 0$ W, $Q_o = 0$ VAr

Test body

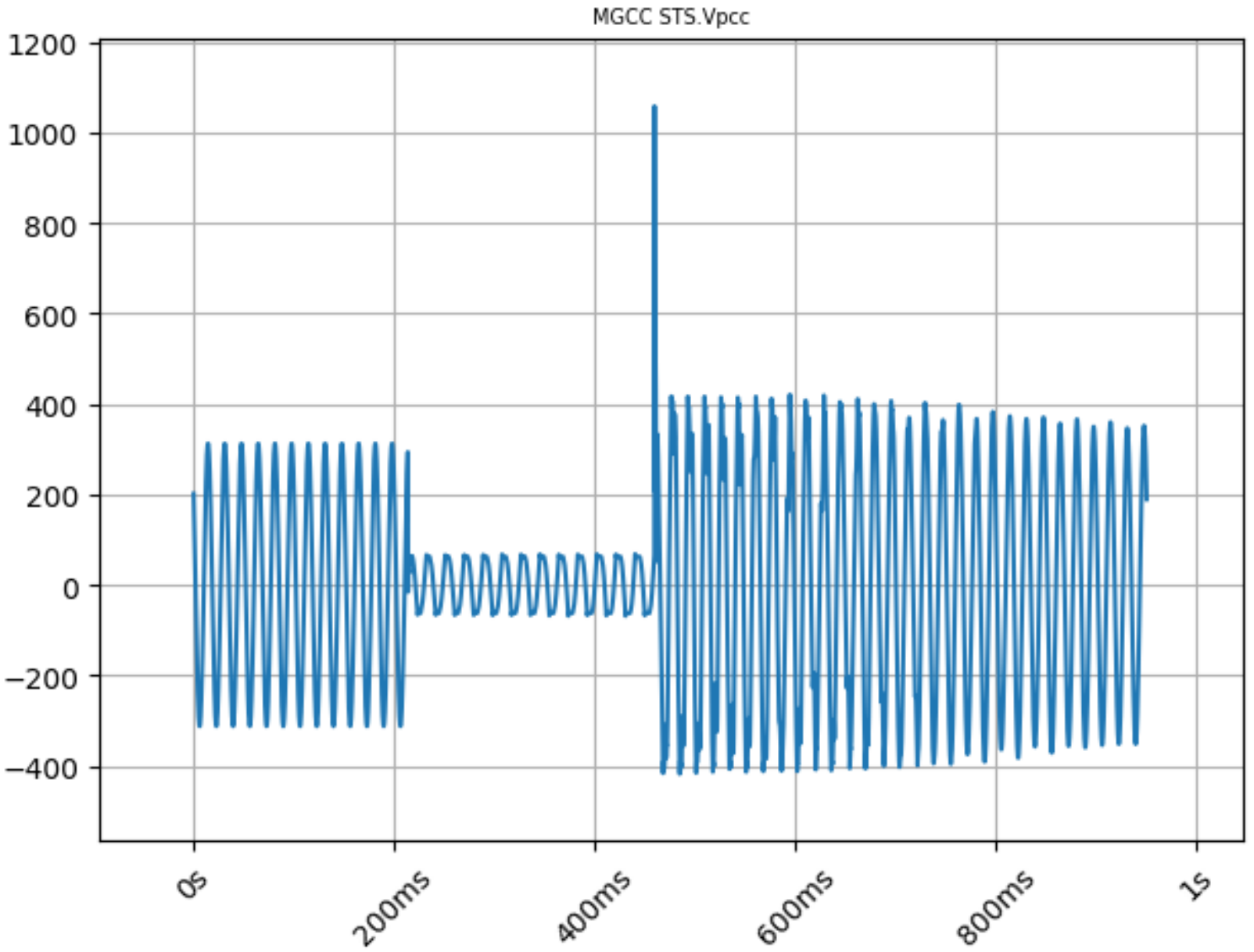
FAIL -> Frequency error = 3.1129608154296875Hz (max = 3Hz)

VSG (regulation of Q_{gap})

Test Suite



- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]



Test body

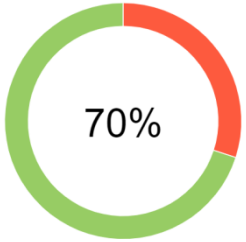
FAIL -> Vmax = 1057.919189453125V (max = 800V)

FAIL -> DER Active power tracking

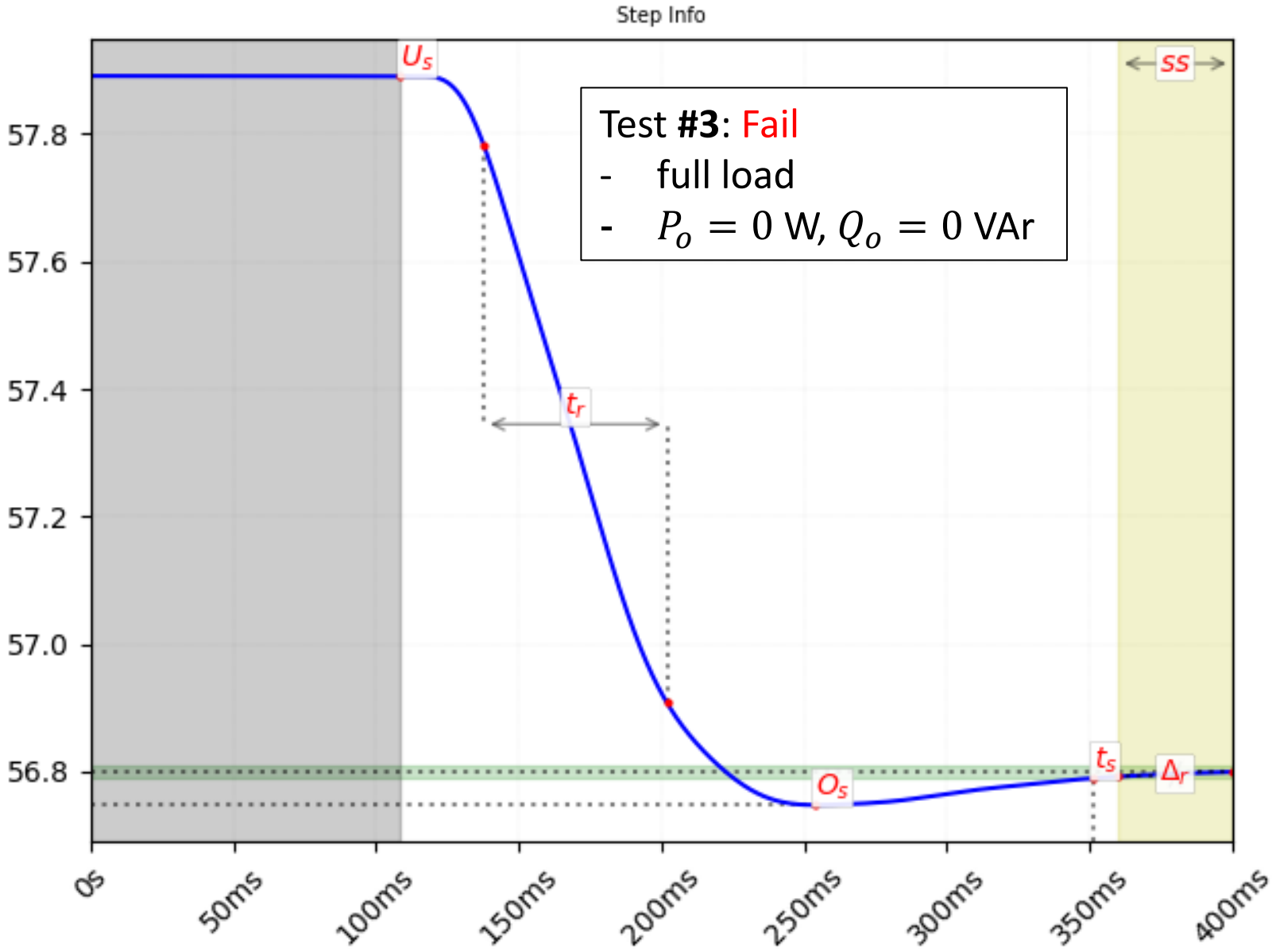
FAIL -> DER Reactive power tracking

VSG (regulation of Q_{poc})

Test Suite



- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]



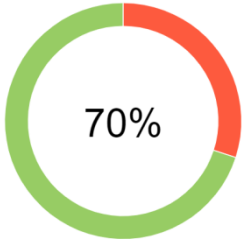
Test **#3**: Fail
- full load
- $P_o = 0$ W, $Q_o = 0$ VAr

Test body

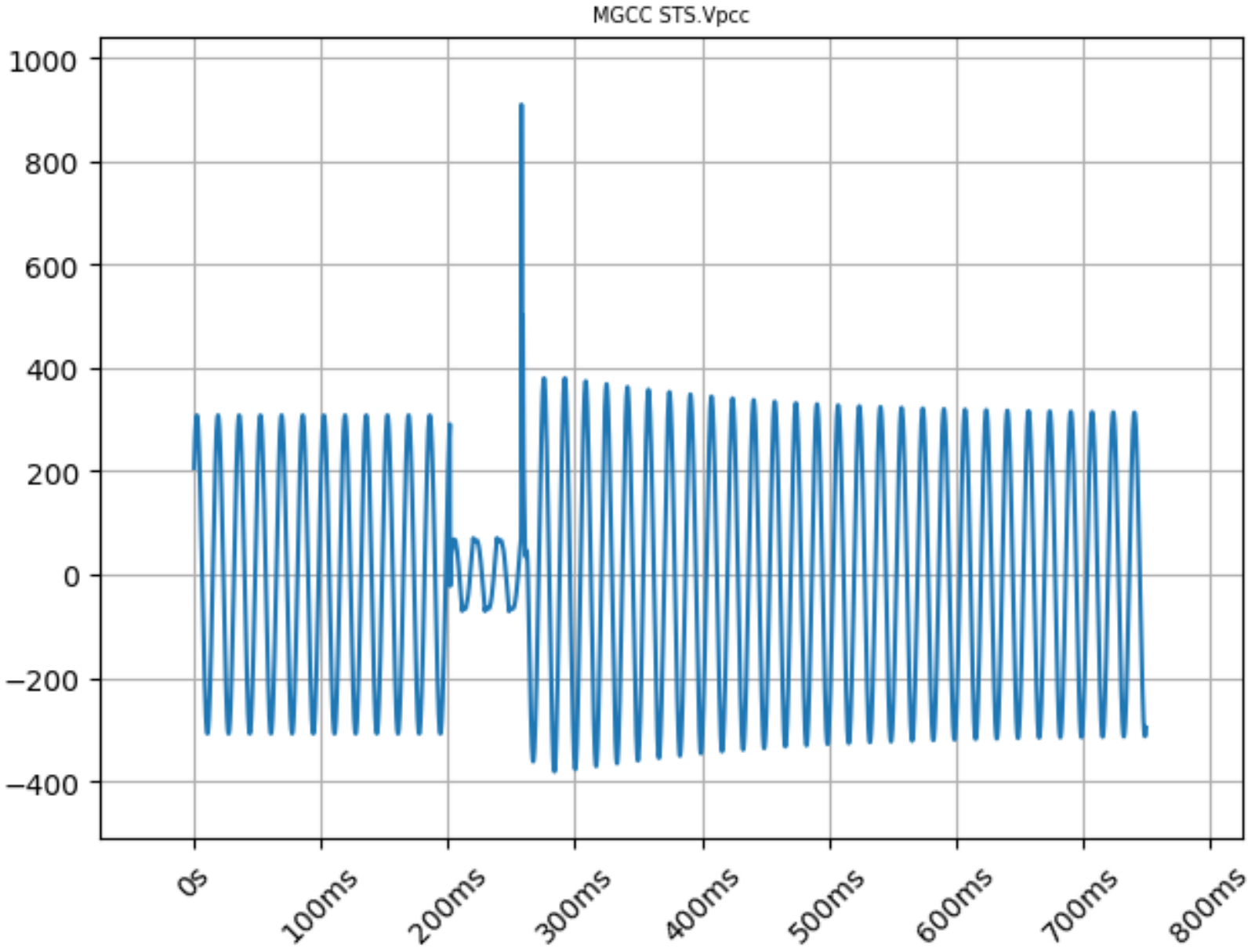
FAIL -> Frequency error = 3.203838348388672Hz (max = 3Hz)

VSG (regulation of Q_{poc})

Test Suite



- test_linear
  - #2 test_tracking[False-True0]
  - #4 test_tracking[False-True1]
  - #1 test_tracking[True-False0]
  - #5 test_tracking[True-False1]
  - #3 test_tracking[True-True]
- test_nonlinear
  - #2 test_tracking[False-True]
  - #1 test_tracking[True-False]
  - #3 test_tracking[True-True]
- test_short
  - #1 test_tracking[0.05]
  - #2 test_tracking[0.25]

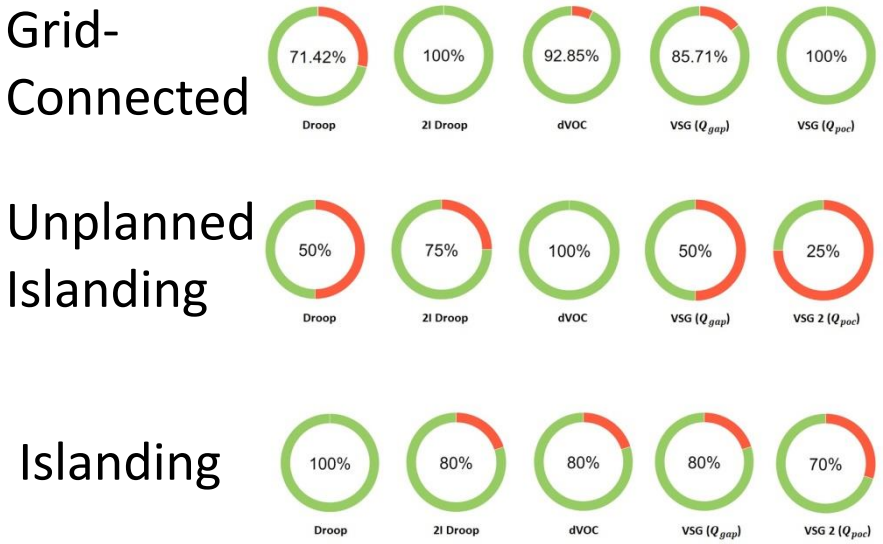


Test body

FAIL -> Vmax = 909.3212890625V (max = 800V)

Summary

- The test-driven design provided a holistic way to evaluate the performance of primary controllers for microgrid point out the strong and weak point of each alternative.
- The Droop controller has:
  - Simple implementation
  - Excellent behavior during short circuit
  - Large reactive power dispatch errors when connected the grid.
- The 2I Droop reduces the droop the steady-state error at the price of penalizing the behavior after the short-circuit.



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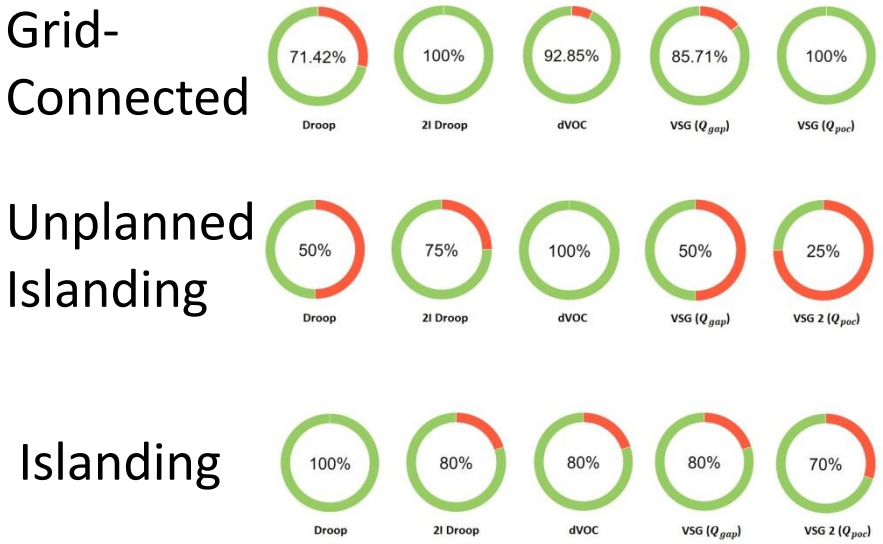
Summary

- The dVOC demonstrated to be a strong candidate for primary controller, just requiring attention for short-circuit case in islanding mode.

- The VSG makes it possible to select the droop characteristic and moment of inertia as in conventional synchronous generator. Again critical point to be addressed is the power sharing after the short-circuit clearing.

- All the files used in this course are available at https://hil.academy/



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Credits

Acknowledgement: This project is the result of an agreement between Fatec / UFSM and Typhoon HIL, Inc.,
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